Digital Power Factor Correction.
Recent approaches with and without current sensor

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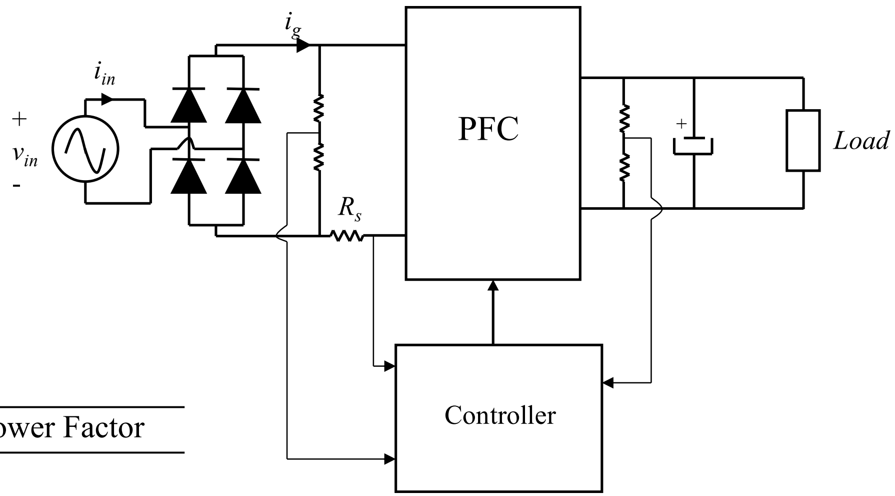
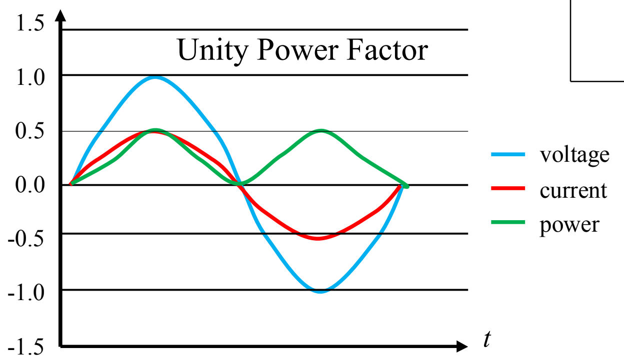
Introduction

- PFC
  - AC-to-DC converters meet power quality standards



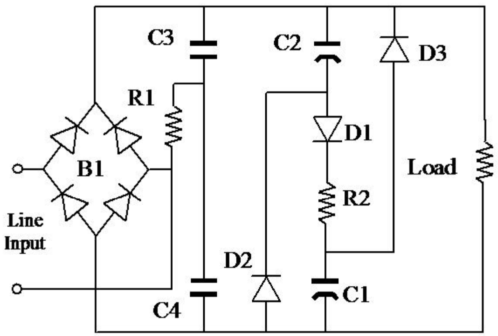


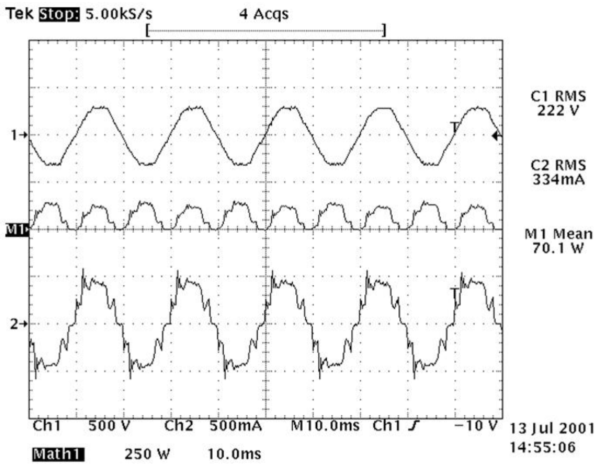
IEC 61000-3-2

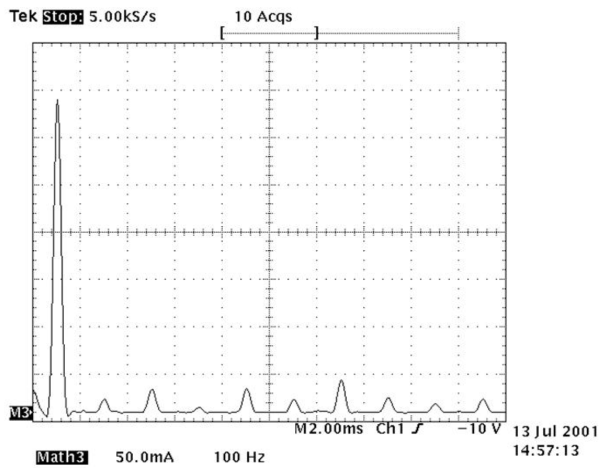
n	Class A (A rms)	Class B (A rms)	Class C (% fun.)	Class A (mA/W)
3	2.3	3.45	30PF	3.4
5	1.14	1.71	10	1.9
7	0.77	1.155	7	1.0
9	0.40	0.60	5	0.5
2	1.08	1.62	2	-
4	0.43	0.645	-	-
6	0.30	0.45	-	-
8<n<40	1.84/n	2.76/n	-	-

Introduction

- Passive Valley-fill circuit
  - Low power applications



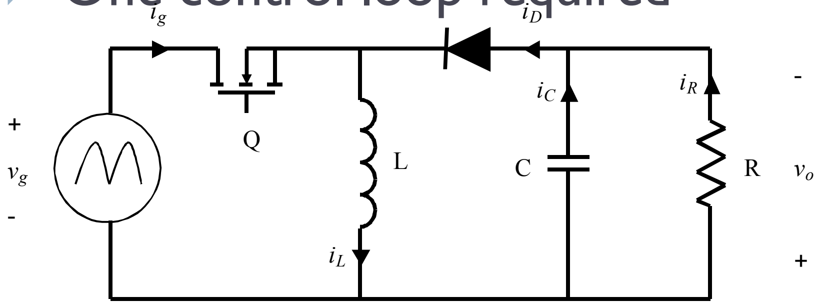




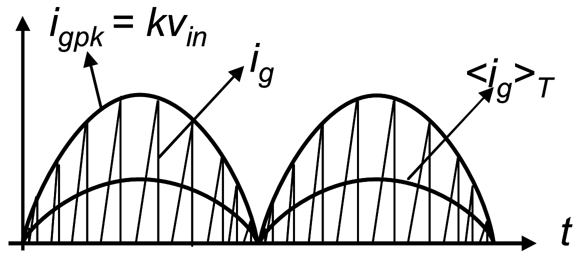
Christian Brañas, Francisco J. Azcondo, Salvador Bracho. Evaluation of an electronic ballast circuit for HID lamps with passive power factor correction. Proc. of The 28th Annual Conference of IEEE Industrial Electronics Society IECON'02. pp.:371-376

Introduction

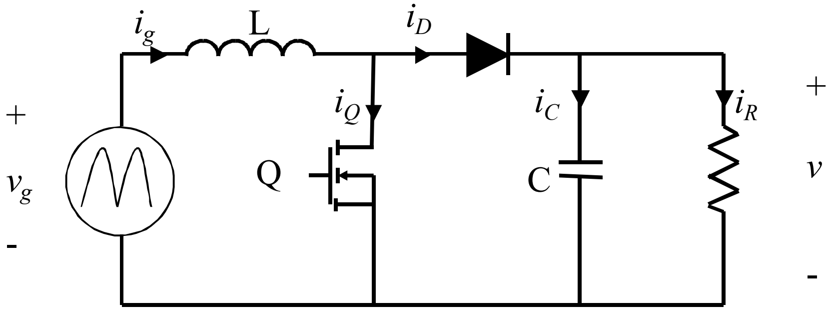
- DCM / CCM-DCM
  - No active current control
  - One control loop required



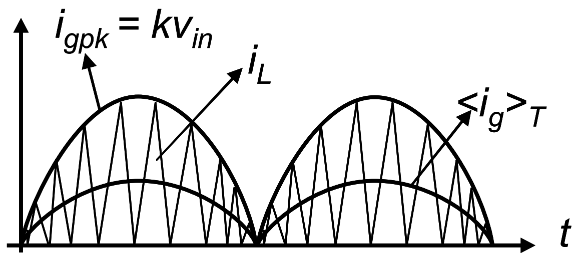
$$i_{gpk} \cong v_g \frac{DT}{L}$$



$$\langle i_g \rangle_T = v_g \frac{D^2 T}{2L}$$



$$i_{gpk} \cong v_g \frac{dT}{L}$$

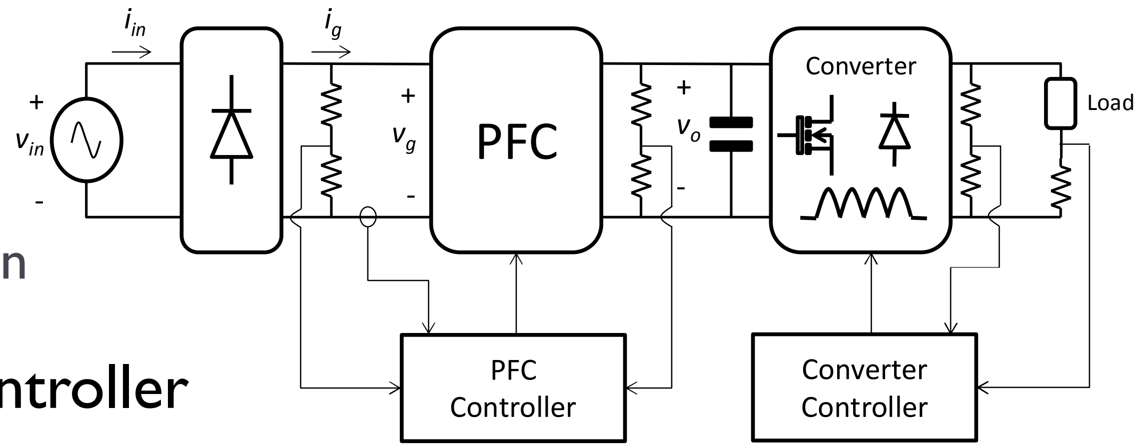


$$\langle i_g \rangle_T \cong v_g \frac{dT}{2L}$$

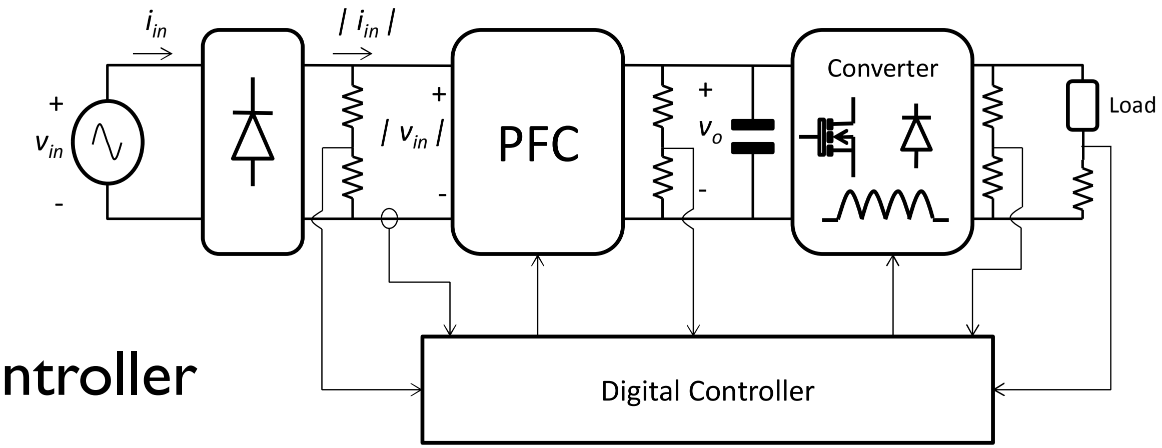
Introduction

- CCM
  - Higher power
  - Lower component stress
  - Lower conduction emission

- Analog controller



- Digital controller

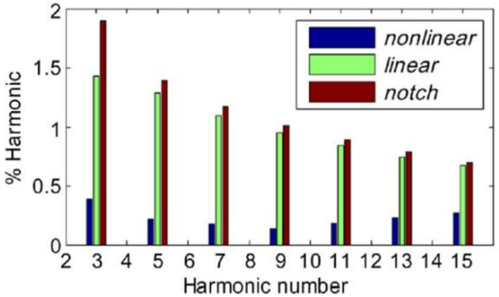


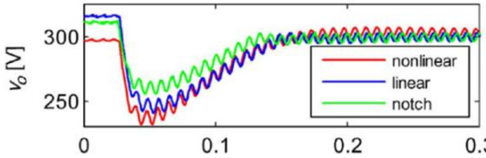
Introduction

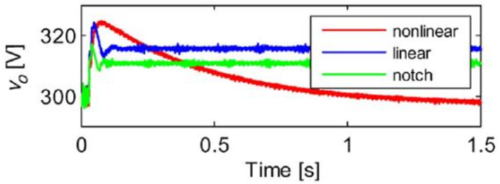
- Benefits of digital circuit capabilities broadly discussed
  - Interaction with other circuits (e.g. multi-phase)
  - Implementation of advanced control techniques (adaptive, non-linear, predictive, multi-mode, improved stability)
  - Programmability, configuration
  - System identification, autotuning
  - Lower number of external passive components, including sensors
  - Higher performance (more variables, complexity, protection, wider input and output ranges, dynamic response)
  - Reduced sensitivity to ripple, noise, temperature, aging, process variation …

Examples of digital controllers

Higher performance



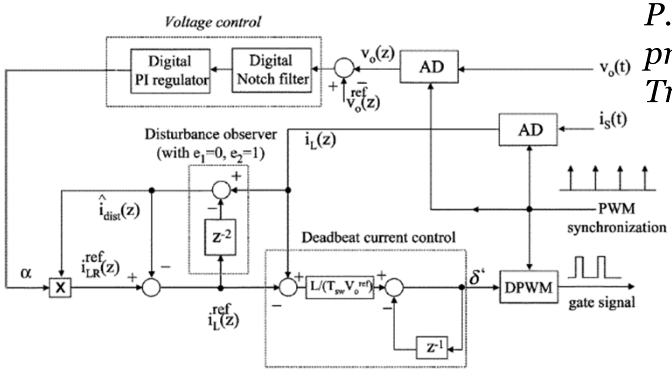




Includes a load estimator

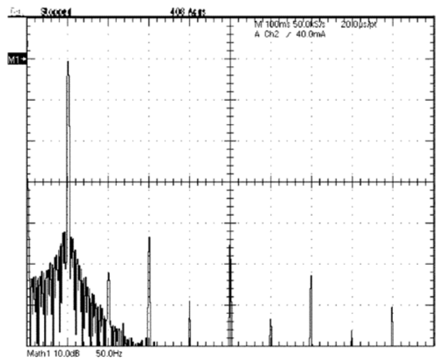
V. Rao, A. Jain, K. Reddy, and A. Behal, "Experimental comparison of digital implementations of single-phase PFC controllers," IEEE Transactions on Industrial Electronics, vol. 55, no. 1, pp. 67 –78, Jan. 2008.

Reduction of measurements



Includes a notch filter

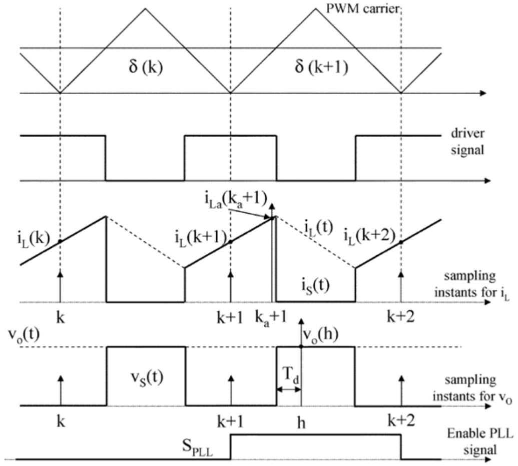
P. Mattavelli, G. Spiazzi, and P. Tenti, "Predictive digital control of power factor preregulators with input voltage estimation using disturbance observers," IEEE Transactions on Power Electronics, vol. 20, no. 1, pp. 140–147, Jan. 2005



All harmonics below 40dB after offset compensation

Examples of digital controllers

Ripple rejection



W. Stefanutti, P. Mattavelli, G. Spiazzi, and P. Tenti, "Digital control of single-phase power factor preregulators based on current and voltage sensing at switch terminals," IEEE Transactions on Power Electronics, vol. 21, no. 5, pp. 1356–1363, Sept. 2006

- Sampling instants for the switch current in the middle of the switch-on time (CCM is assumed)
- Sampling instants for the switch voltage during off-time and synchronized with the estimated peak input voltage
- PI current controller derived from a given stability condition
- Input voltage estimated with the integral part of the current controller

Improve stability

$$\langle i_L \rangle = \frac{v_g}{R_e} = \frac{V_o}{R_e}(1-d)$$

$$R_e = \frac{V_{g,rms}^2}{P}$$

$$u = \frac{R_e}{V_o}$$

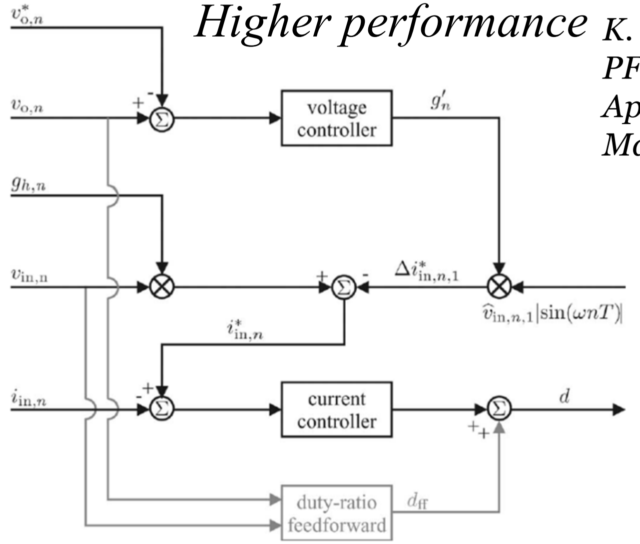
Digitalized control law $\longrightarrow$ $d[n] = 1 - u \cdot i_L[n]$

- Sampling instants for the switch current in the middle of the switch-on time (*d[n-1]* > 0.5) or switch off time (*d[n-1]* < 0.5)
- Modification for stability at light loads (d_{max} limited)
- ΣΔ modulator to improve the resolution of *u*

B. A. Mather and D. Maksimovic, "A simple digital power factor correction rectifier controller," IEEE Transactions on Power Electronics, vol. 23, no. 1, pp. 9 –19, Jan 2010

Examples of digital controllers

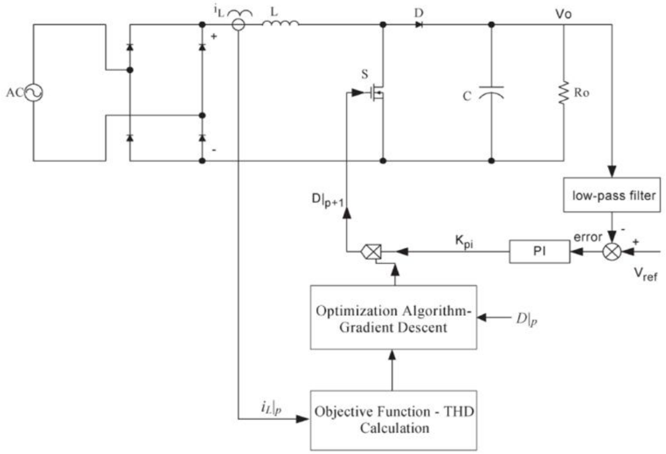
Higher performance



K. De Gusseme, W. Ryckaert, D. Van de Sype, J. Gijselen, and J. Melkebeek, "A boost PFC converter with programmable harmonic resistance," in Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005., vol. 3, Mar. 2005, pp. 1621 –1627

- Feedforward maintain resistance at high frequency
- Output voltage controller affects first harmonic resistance
- Constant higher harmonic resistance

$$d_{ff} = 1 - \frac{v_{in}}{v_o}$$



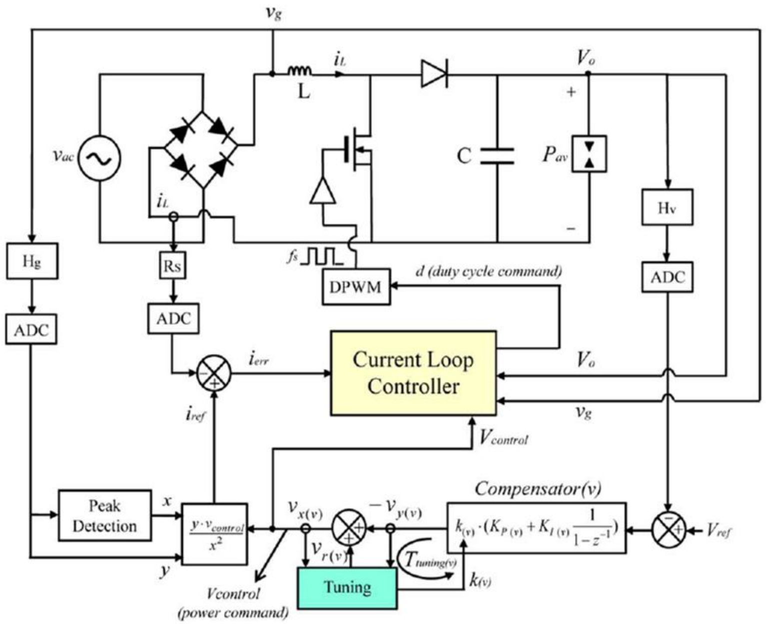
Circuit simplification

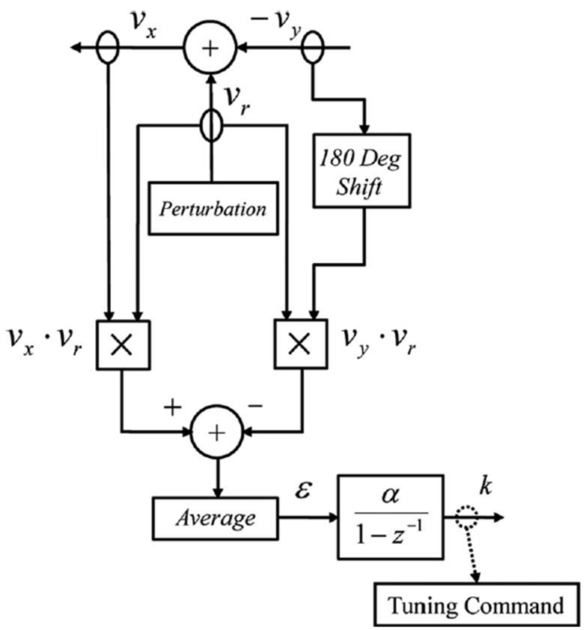
- Duty-cycles calculated in advance
- Switching frequency not dependent on DSP speed
- Algorithm to minimize THDi

W. Zhang, G. Feng, Y.-F. Liu, and B. Wu, "New digital control method for power factor correction," IEEE Transactions on Industrial Electronics, vol. 53, no. 3, pp. 987 – 990, Jun. 2006

Examples of digital controllers

System identification





S. Moon, L. Corradini, and D. Maksimovic, "Autotuning of digitally controlled boost power factor correction rectifiers," IEEE Transactions on Power Electronics, vol. 26, no. 10, pp. 3006 –3018, Oct. 2011

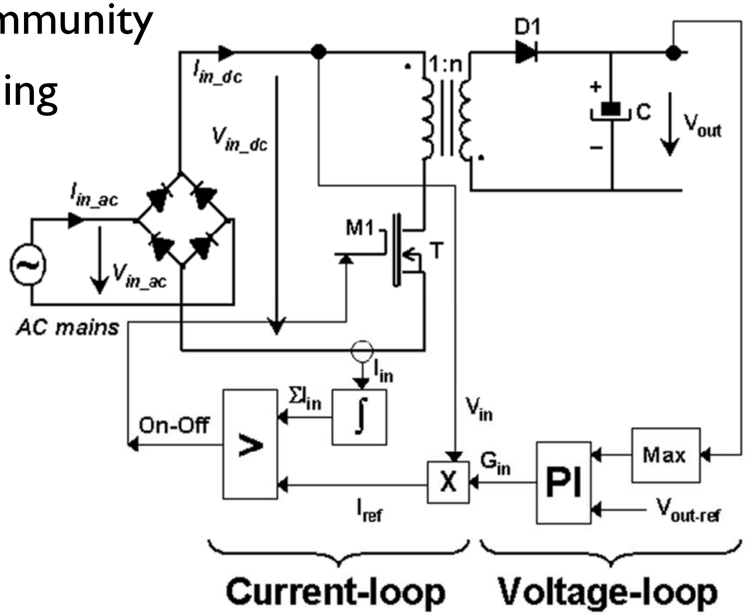
Digital controllers with current sensor

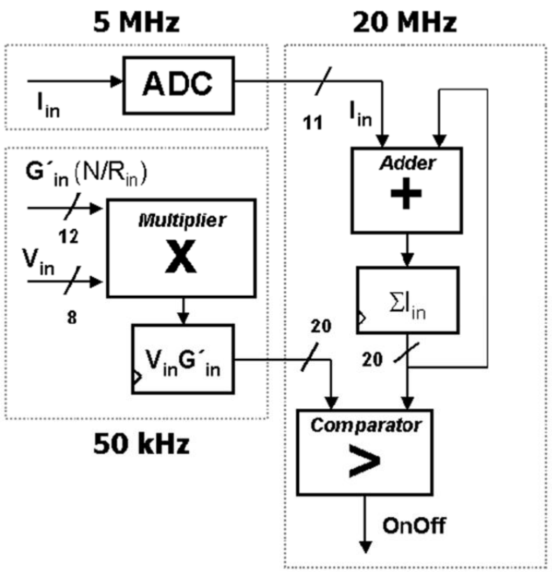
- Current acquisition
  - Fast and high resolution ADC
    - Expensive
    - Filter required
  - One sample *i[k]* = <*i*>
    - Poor noise immunity
    - Accurate timing

Circuit simplification

- Only *dT* is required to compute <*i*>
- Advantages of concurrency

A. de Castro, P. Zumel, O. Garcia, T. Riesgo, and J. Uceda, "Concurrent and simple digital controller of an AC/DC converter with power factor correction based on an FPGA," IEEE Transactions on Power Electronics, vol. 18, no. 1, pp. 334 – 343, Jan. 2003

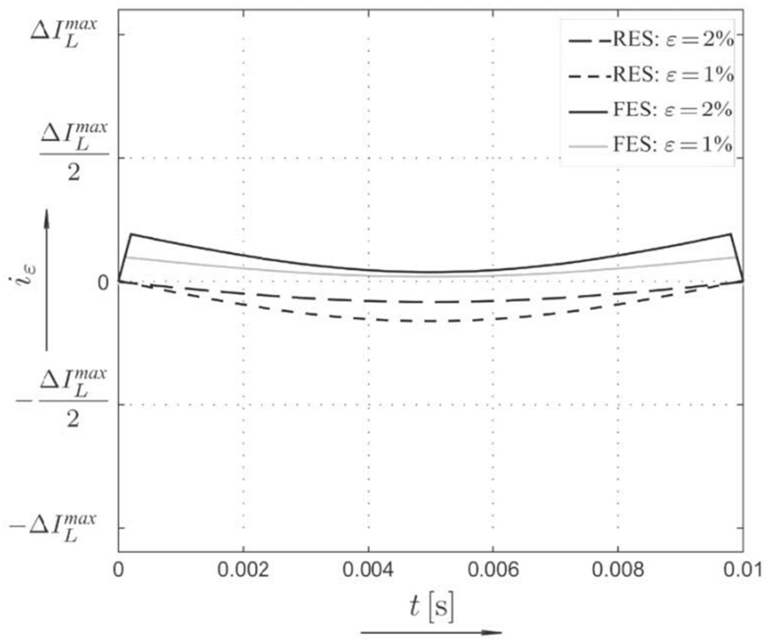


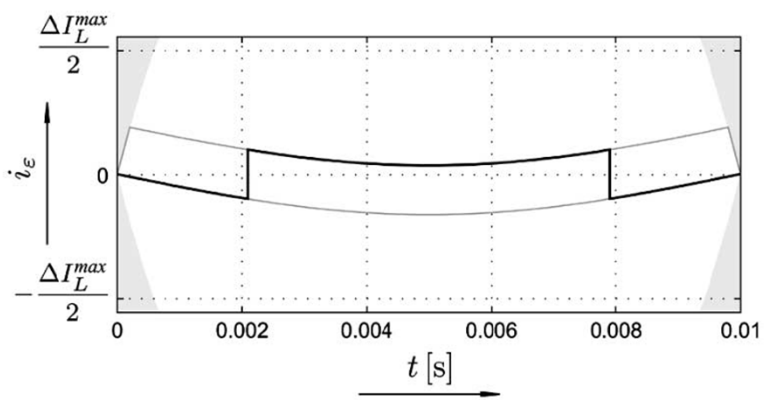


Digital controllers with current sensor

- One sample per switching period
- Noise caused by sampling delay
- Alternative edge sampling
  - Rising edge sampling (large duty ratio)
  - Falling edge sampling (small duty ratio)

Improve noise immunity



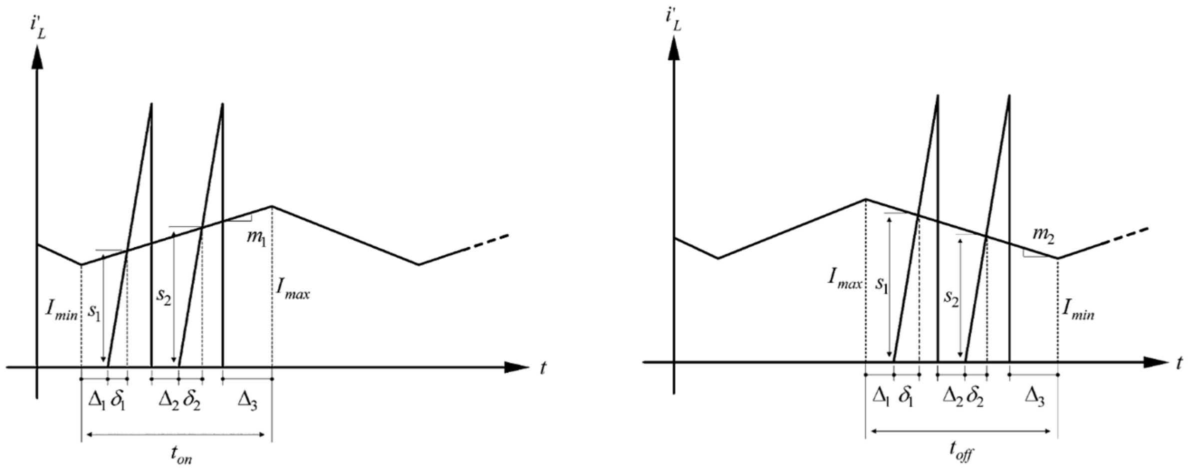


D. Van de Sype, K. De Gusseme, A. Van den Bossche, and J. Melkebeek, "A sampling algorithm for digitally controlled boost PFC converters," IEEE Transactions on Power Electronics, vol. 19, no. 3, pp. 649 – 657, May. 2004

Digital controllers with current sensor

Circuit simplification

- No ADC device
- No low pass filter required
- Also computes input voltage using synchronizing signal
- No synchronization to measure output voltage

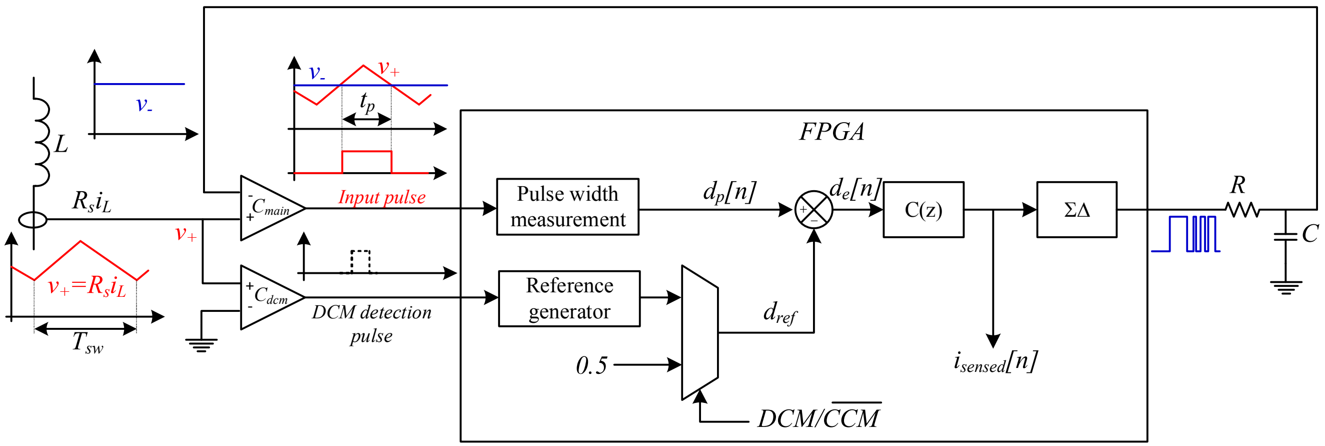


K. Hwu, H. Chen, and Y. Yau, "Fully digitalized implementation of PFC rectifier in CCM without ADC," IEEE Transactions on Power Electronics, vol. 27, no. 9, pp. 4021–4029, Sept. 2012

Digital controllers with current sensor

Circuit simplification

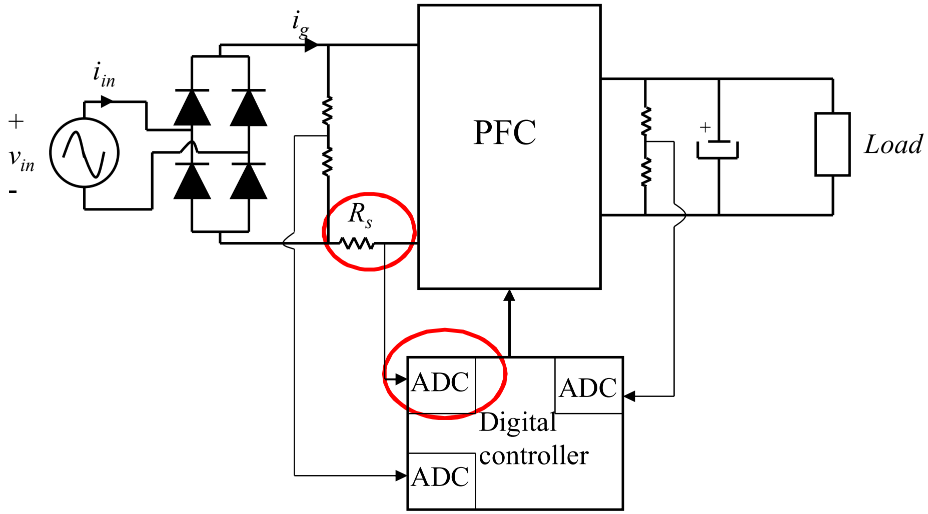
- No ADC device
- Adapted for CCM and DCM

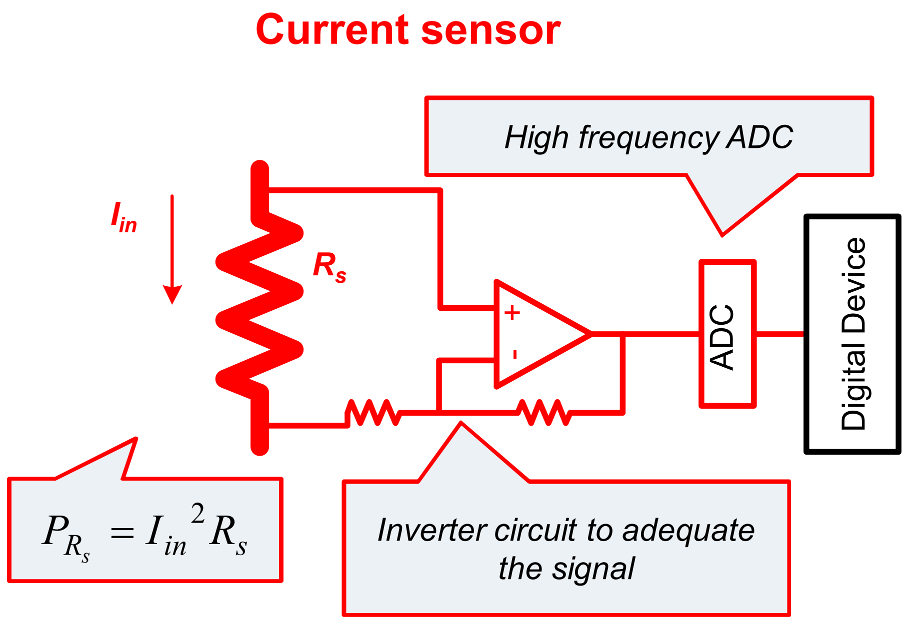


M. Rodriguez, V. Lopez, F. Azcondo, J. Sebastian, and D. Maksimovic, "Average inductor current sensor for digitally controlled switched-mode power supplies," IEEE Transactions on Power Electronics, vol. 27, no. 8, pp. 3795 –3806, Aug. 2012.

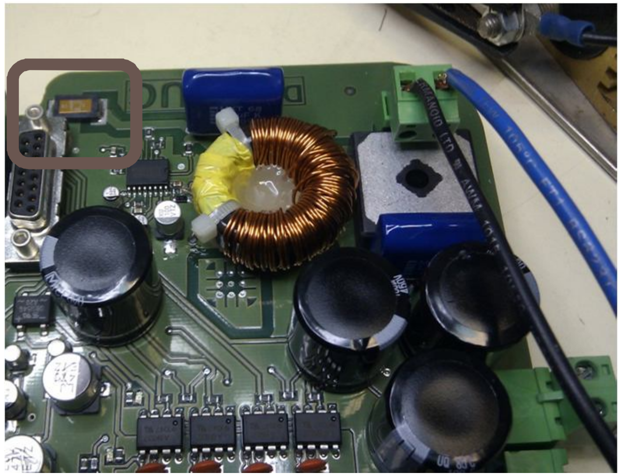
Digital controllers without current sensor

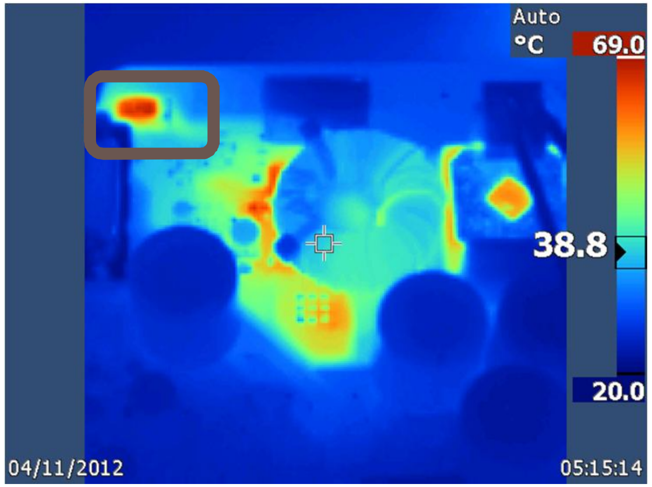
- Motivation





Digital controllers without current sensor





V_{in} (V)	V_o (V)	P_o (W)	I_{in} (A)	P_{Rs} (W)
120	400	320	2.68	1.44
120	400	480	4.03	**3.24**
120	400	640	5.38	**5.79**
120	400	800	6.74	**9.09**
120	400	960	8.11	**13.15**
230	400	320	1.39	0.39
230	400	480	2.09	0.87
230	400	640	2.79	**1.56**
230	400	800	3.49	**2.43**
230	400	960	4.19	**3.51**
230	400	1120	4.89	**4.78**

-CCM PFC is used high power solutions (200 – 1000 W)

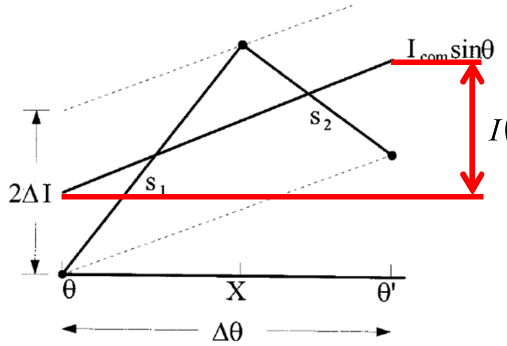
-The designer has to achieve a voltage threshold drop in the current sensor at nominal power

-$R_s \approx 0.2\ \Omega$

-Table with the estimated power losses in the current sensor for different output loads and American/European grid

Power electronics Lab. UC. 2012

Digital controllers without current sensor



$$I(\sin\theta' - \sin\theta) = s_1(X-\theta) + s_2(\theta' - X)$$

Y.-K. Lo, H.-J. Chiu, and S.-Y. Ou, "Constant-switching-frequency control of switch-mode rectifiers without current sensors," IEEE Transactions on Industrial Electronics, vol. 47, no. 5, pp. 1172 –1174, Oct. 2000

$$d(\theta) = \frac{X-\theta}{\Delta\theta} = 1 + \frac{\omega L I}{V}\frac{d\sin\theta}{d\theta} - \frac{v_g}{V}$$

$$d'(\theta) = 1 - d(\theta) = \frac{v_g}{V} - \frac{\omega L I}{V}\frac{d\sin\theta}{d\theta}$$

$v_g \Rightarrow$ measured

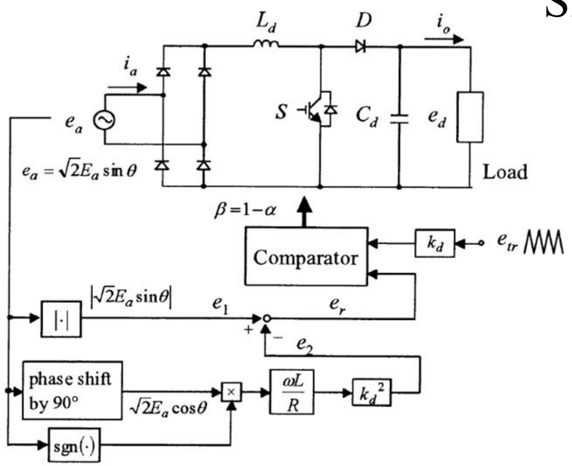
$V \Rightarrow$ measured

$\dfrac{d\sin\theta}{d\theta} \Rightarrow$ computed from v_g

$\omega L \Rightarrow$ constant

$I \Rightarrow$ results from feedback

Similarly



$$d'(\theta) = \frac{\sqrt{2}}{k_d}\sin(\omega t) - \sqrt{2}\left(\frac{\omega L}{R_d}\right)k_d\cos(\omega t)$$

$$k_d = \frac{V}{V_{g,rms}} \text{(limited by the controllable region)}$$

$$I_{rms} = \frac{V^2}{R_d V_{g,rms}}$$

$v_g \Rightarrow$ measured

$V \Rightarrow$ not measured, imposed by k_d

$\cos\theta \Rightarrow$ computed from v_g

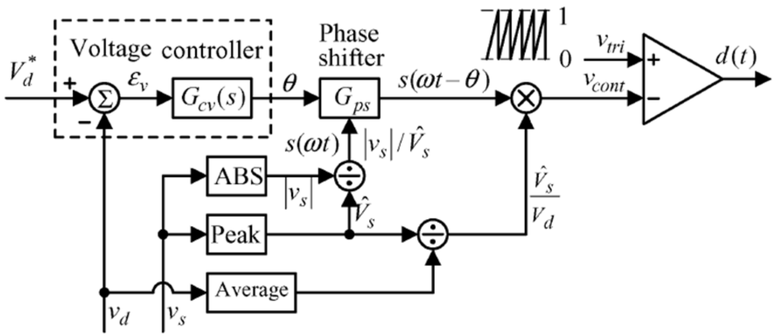
$\dfrac{\omega L}{R_d} \Rightarrow$ small to accept load variation

T. Ohnishi and M. Hojo, "DC voltage sensorless single-phase PFC converter," IEEE Transactions on Power Electronics, vol. 19, no. 2, pp. 404–410, March 2004

Digital controllers without current sensor

Also, similar approach using

$d = 1 - \frac{V_{g,peak}}{V} \sin(\omega t - \theta)$, with θ as the control variable



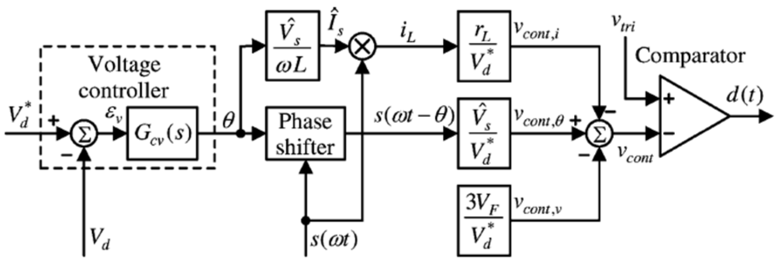
$$L\frac{di}{dt} = V_{g,peak}\sin(\omega t) - (1-d)V$$

$$L\frac{di}{dt} = V_{g,peak}\sin(\omega t) - V_{g,peak}\sin(\omega t - \theta)$$

with θ small, $L\frac{di}{dt} \cong V_{g,peak}\theta\cos(\omega t)$, and $i = \frac{V_{g,peak}\theta}{\omega L}\sin(\omega t)$

H.C. Chen "Duty phase control for single-phase boost-type SMR" IEEE Trans. on Power Electron. , vol. 23, no. 4. Pp. 1927-1934, Jul. 2008

Taking V_F and r_L into account



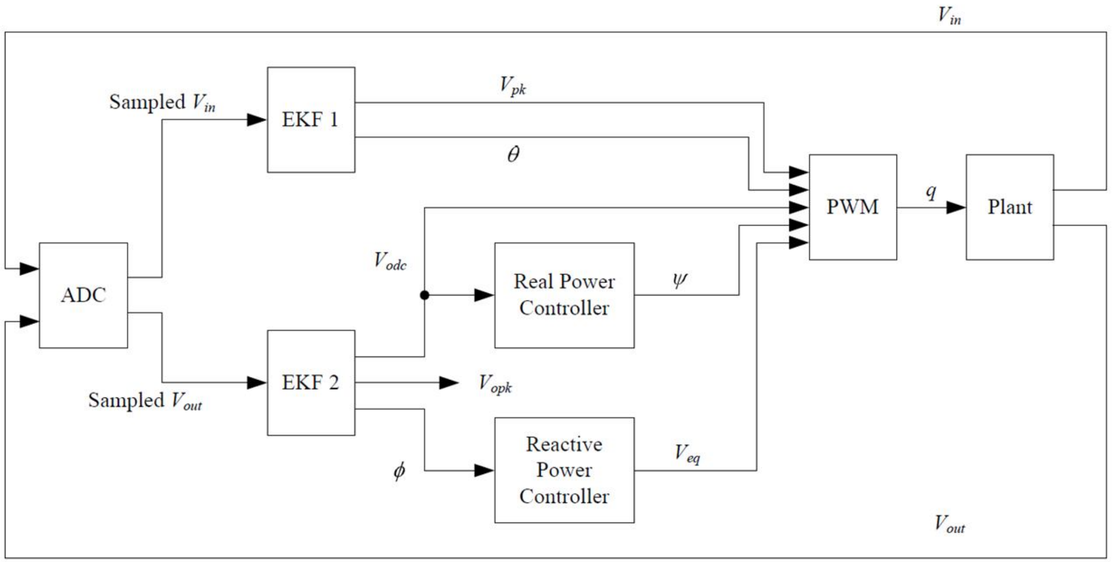
H.C. Chen, "Single-loop current sensorless control for single-phase boost-type smr," IEEE Transactions on Power Electronics, vol. 24, no. 1, pp. 163 –171, Jan. 2009

Artificial v_g using LUT to gain immunity under distorted input voltage

H.C. Chen, C.-C. Lin, and J.-Y. Liao, "Modified Single-Loop Current Sensorless Control for Single-Phase Boost-Type SMR With Distorted Input Voltage," IEEE Transactions on Power Electronics, vol. 26, no. 5, pp. 1322 –1328, May 2011

Digital controllers without current sensor

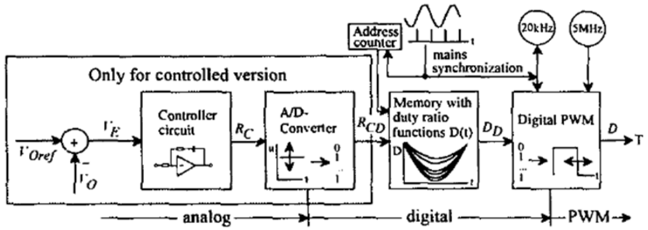
- Replace the sensor by an observer defined by an Extended Kalman Filter
  - Feedback to compensate estimation errors
  - EKF 1 obtain v_g (sinusoidal waveform is assumed)
    - Analog and quantization noise are reduced
  - EKF2 defines the plant (observer) and is adjusted by comparing with v_{out}
    - Amplitude and ripple phase are used
    - Deadbeat control



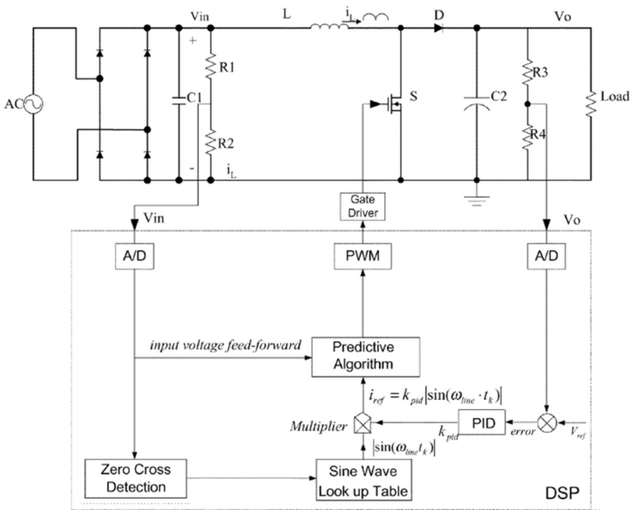
J. Kimball and P. Krein, "A current-sensorless digital controller for active power factor correction control based on kalman filters," in Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, 2008. APEC 2008., Feb. 2008, pp. 1328–1333.

Digital controllers without current sensor

- Pre-calculated duty-cycle
  - Duty-cycles stored in a digital memory and recalled by a counter. Synch with v_g
    - Good results with just 4 bits or more
    - Uncontrolled (no v_g nor v_o sensing) and controlled version (only v_o sensing)



I. Merfert, "Stored-duty-ratio control for power factor correction," in Fourteenth Annual Applied Power Electronics Conference and Exposition, 1999. APEC '99., vol. 2, Mar. 1999, pp. 1123–1129



- Predictive algorithm with $\Delta\, v_g$ feedforward compensation to account for harmonics
- Modified to take into account Δv_o, r_L, r_{on}

$$d[k]=\frac{V_{o,ref}-v_g[k]}{V_{o,ref}}+\frac{\left(i_{ref}[k+1]-i_{ref}[k]\right)\frac{L}{T_s}}{V_{o,ref}}$$

$$i_{ref}[k]=v_{PID}\sin(\omega t_k)$$

$$d_{update}[k]=d[k]+\Delta d[k]$$

$$\Delta d[k]=\frac{\Delta v_g}{V_{o,ref}}$$

W. Zhang, G. Feng, Y.-F. Liu, and B. Wu, "A digital power factor correction (PFC) control strategy optimized for DSP," IEEE Transactions on Power Electronics, vol. 19, no. 6, pp. 1474–1485, Nov. 2004.

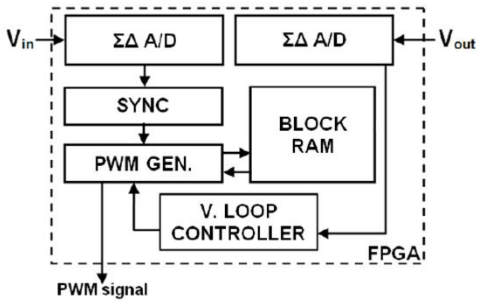
Digital controllers without current sensor

Pre-calculated duty-cycle

- Experimental acquisition of gate-drive signal sequences for different load conditions
- Operation in programming (with sensor) and programmed (without sensor) modes

A. Finazzi, L. de Freitas, J. Vieira, E. Coelho, V. Farias, and L. Freitas, "Currentsensorless PFC Boost converter with preprogrammed control strategy," in IEEE International Symposium on Industrial Electronics (ISIE), 2011, June 2011, pp. 182 –187

- Same technique as in previous slide to calculate the pre-stored duty cycles
- Implementation in FPGA including ΣΔ ADCs

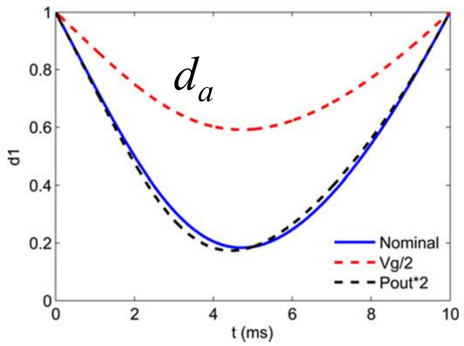


A. Garcia, A. de Castro, O. Garcia, and F. Azcondo, "Pre-calculated duty cycle control implemented in FPGA for power factor correction," in 35th Annual Conference of IEEE Industrial Electronics, 2009. IECON '09., Nov. 2009, pp. 2955 –2960

Digital controllers without current sensor

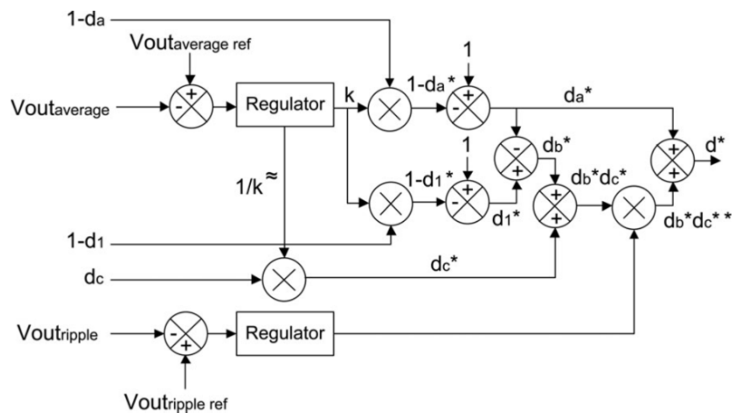
Pre-calculated duty-cycle

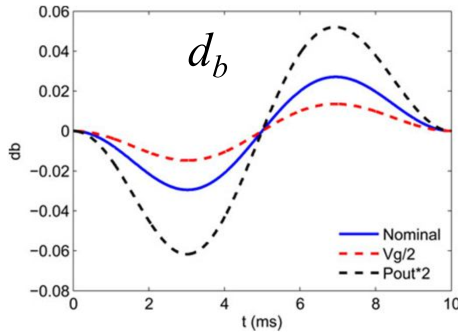
- Pre-calculated duty-cycles divided into three components, d_a, d_b, d_c
- Single ADC for v_o extracting mean value and ripple, v_g comparator for synchronization
- $1-d_a$, $1-d_1$ and d_c values stored in a memory (for nominal v_g and load)

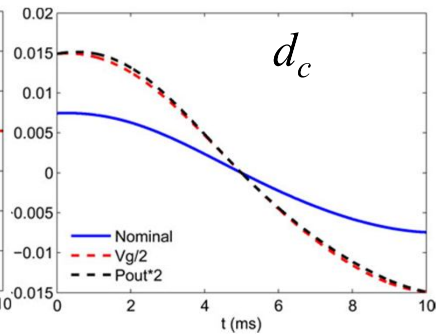


$$d_a[k]=\frac{V_{o,av}-v_g[k]}{V_{o,av}} \qquad d_c[k]=\frac{\left(i_{ref}[k+1]-i_{ref}[k]\right)\frac{L}{T_s}}{V_{o,av}}$$

$$d_1[k]=\frac{v_o[k]-v_g[k]}{v_o[k]} \qquad d_b[k]=d_1[k]-d_a[k]$$



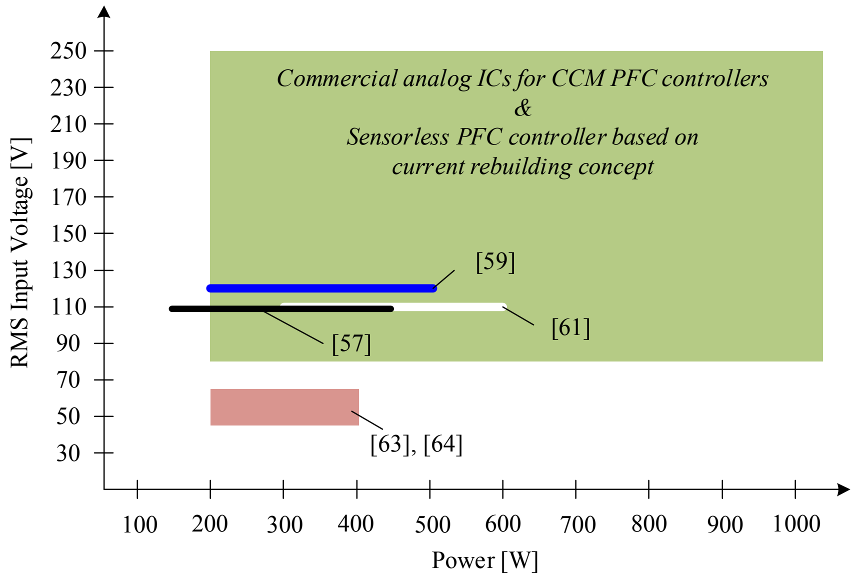




A. Sánchez, A. de Castro, V.M. López, F.J. Azcondo, J. Garrido "Single ADC Digital PFC Controller Using Precalculated Duty Cycles," IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 996–1005, Feb. 2014

UC proposal

- Current sensorless proposals work better with
  - Large L
  - Low f_{sw}
  - Limited v_g range (frequency and amplitude)
  - Limited load range
- Affected by
  - v_g distortion at different degree
  - Parasitic elements
    - R_{on}, R_L, v_d
    - Delays
      - ADC
      - Drivers



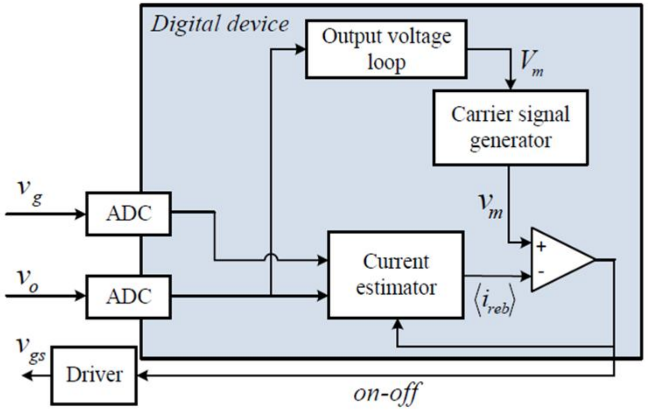
UC proposal

- Universal solution if CCM
  - Observer inherited from the HIL concept
  - Non-linear controller
  - Non-dependence on *L*
  - Broad load range
  - Universal v_g (conventional grid or avionics)
  - Full compensation of the estimation errors
  - Resistor emulator and low THDi solutions with distorted v_g
  - No reconfiguration or tuning is required
  - FPGA implementation

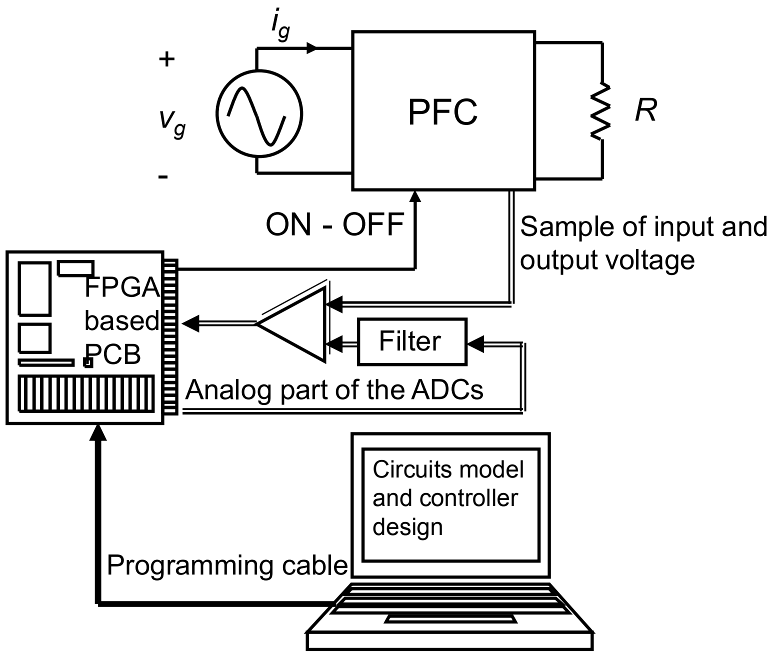
Design framework

- Schematic of the development hardware

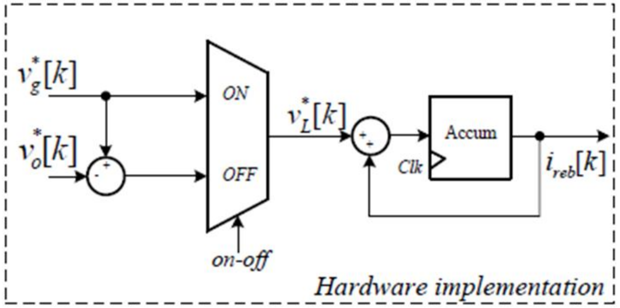
•Test bench
1. Behavioral model of the power converter
    1. Inductor model
2. PFC controller and ADC (for synthesis)
    1. ADC for vg
    2. ADC for vo
    3. Current estimator (observer)
    4. NLC for the PFC
    5. Voltage controller
3. Behavioral model analog part of the ADC



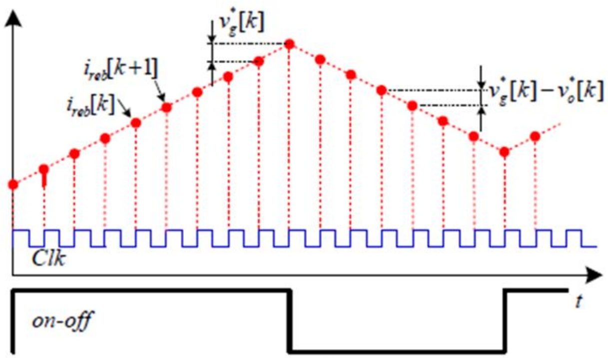
Precedent "*hardware in the loop*"



Current estimation



(a)



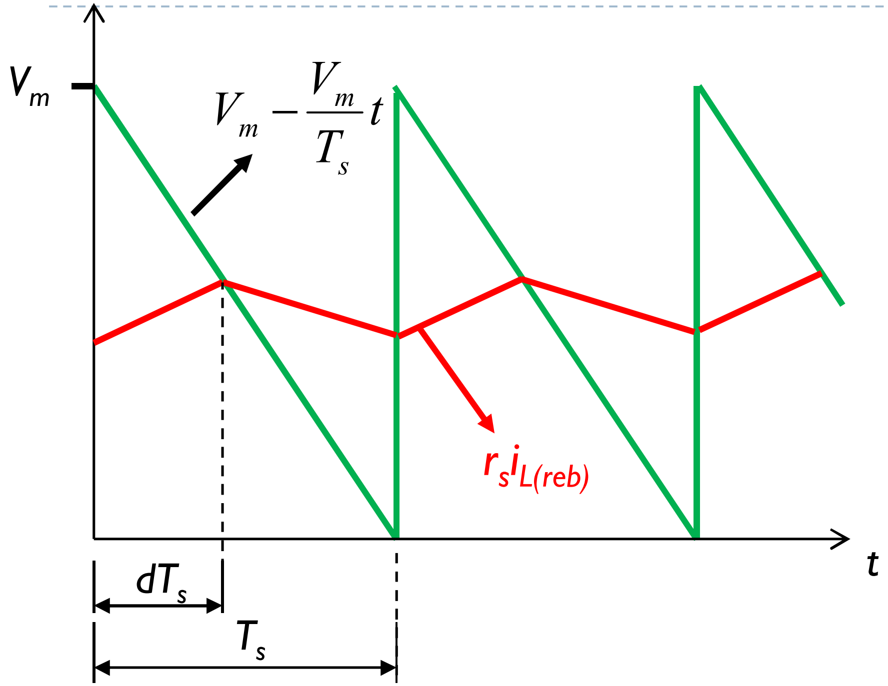
(b)

- Input current estimated with v_g and v_o.
- *Clk* determines the calculation speed.

$$i_L(k+1) = i_L(k) + \frac{v_{in}}{L}\Delta t \qquad i_L(k+1) = i_L(k) + \frac{v_{in} - v_o}{L}\Delta t$$

F. J. Azcondo, A. de Castro, V. M. López and O. García, "Power factor correction without current sensor based on digital current rebuilding", IEEE Transactions on Power Electronics, June 2010.

Non-linear current control

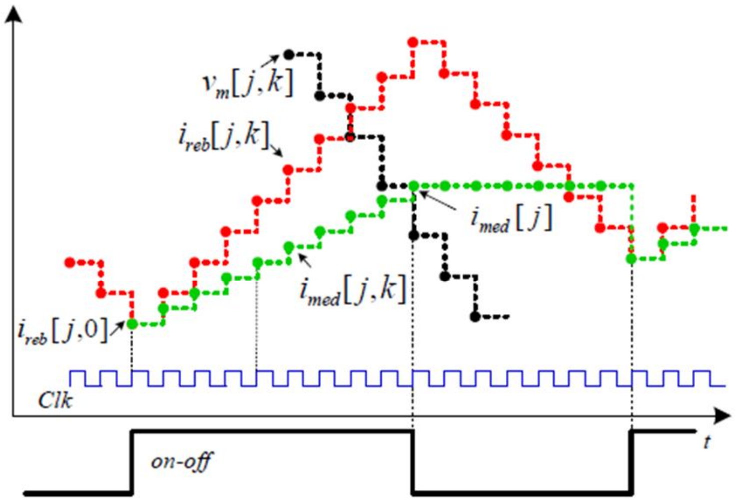


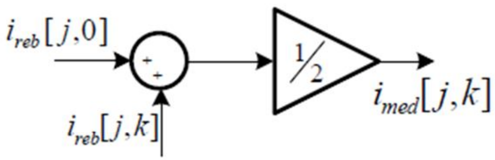
- Control no lineal (NLC) *Peak-current nonlinear carrier control.*
- V_m se obtiene del lazo de tensión.
- El resultado es corrección del factor de potencia en CCM.

Boost	$V_m - V_m \frac{t}{T_s} = r_s i_L$	$V_m(1-d) = r_s i_{Lpk}$	$V_o = \frac{\lvert v_g \rvert}{1-d}$	$i_{Lpk} \approx \lvert v_g \rvert$
SEPIC	$V_m - V_m \frac{t}{T_s} = r_s i_L \frac{t}{T_s}$	$V_m \frac{(1-d)}{d} = r_s i_{Lpk}$	$V_o = \lvert v_g \rvert \frac{d}{1-d}$	$i_{Lpk} \approx \lvert v_g \rvert$

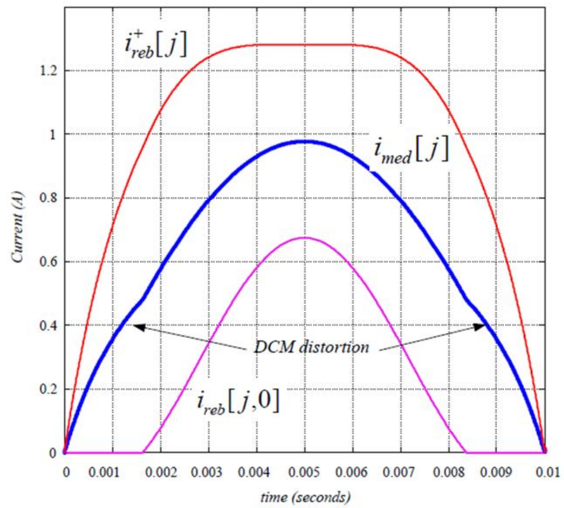
Different references by Prof. S. Cuk on OCC , by Profs. R. Erickson, D. Maksimovic & R. Zane on NLC, by K. Smedley on CCM - PFC and implementations by Prof. G. Spiazzi and J. Sebastián (VCCR), entre otros.

Non-linear current control

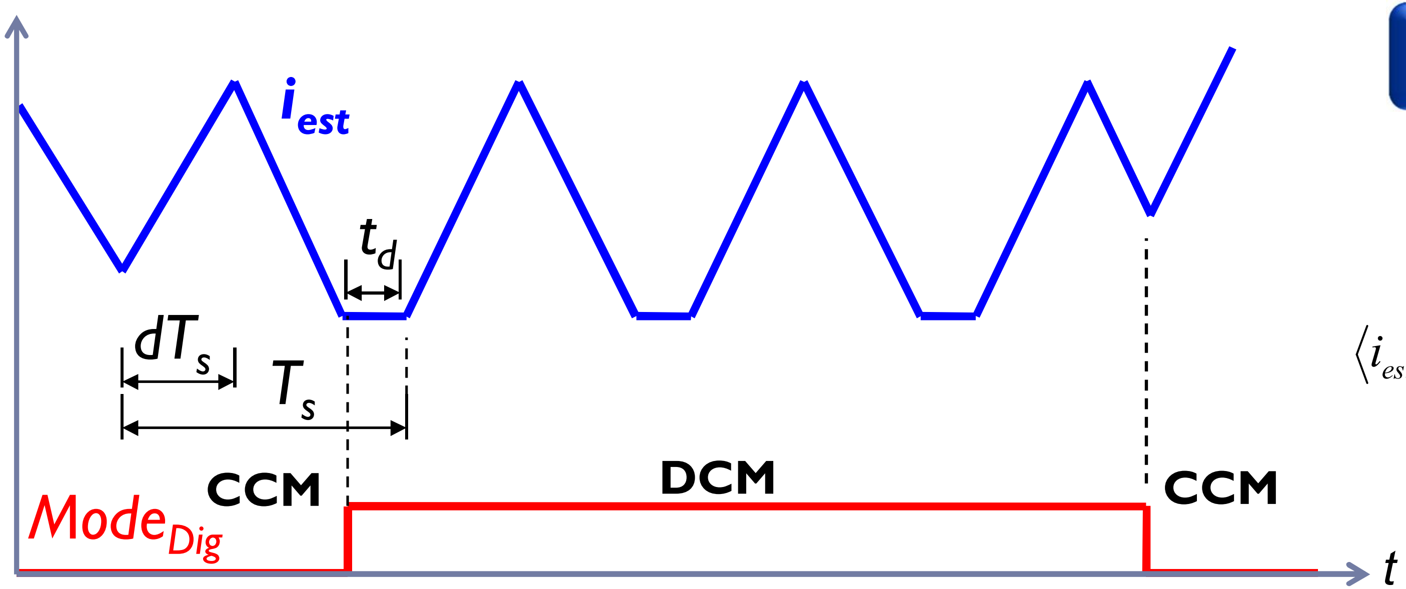




- NLC applied to averaged estimated input current



Non-linear current control

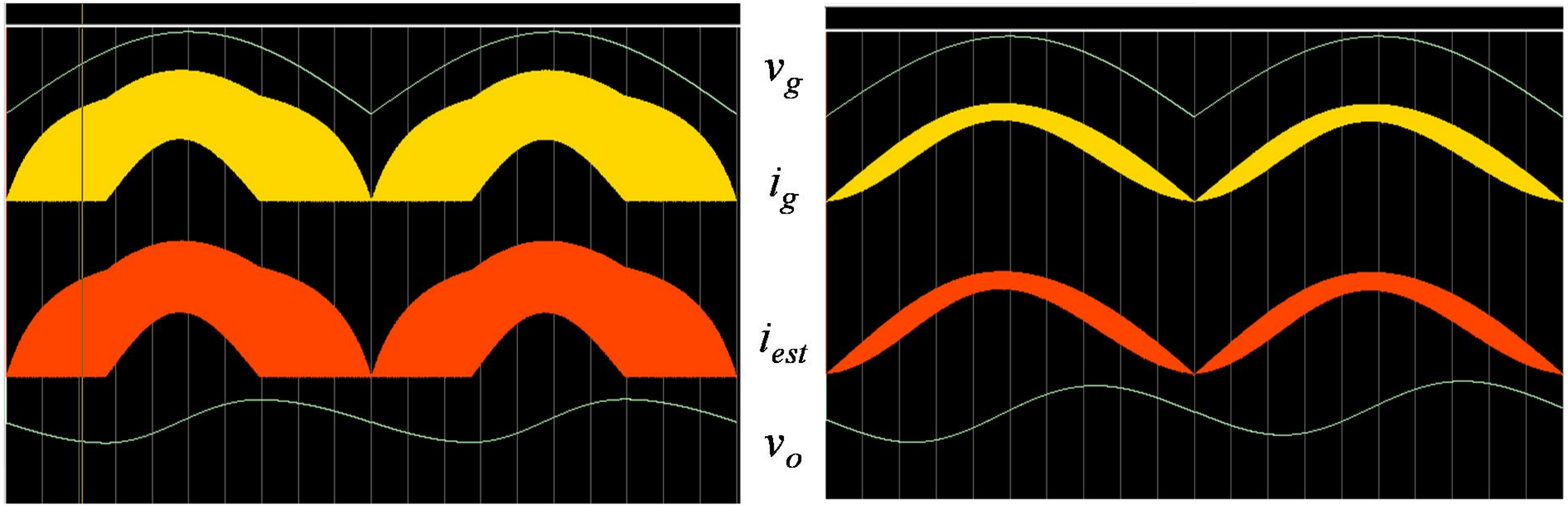


DCM

$$\langle i_{est} \rangle_T = \frac{i_{estpk}}{2}\left(1 - \frac{t_d}{T}\right)$$

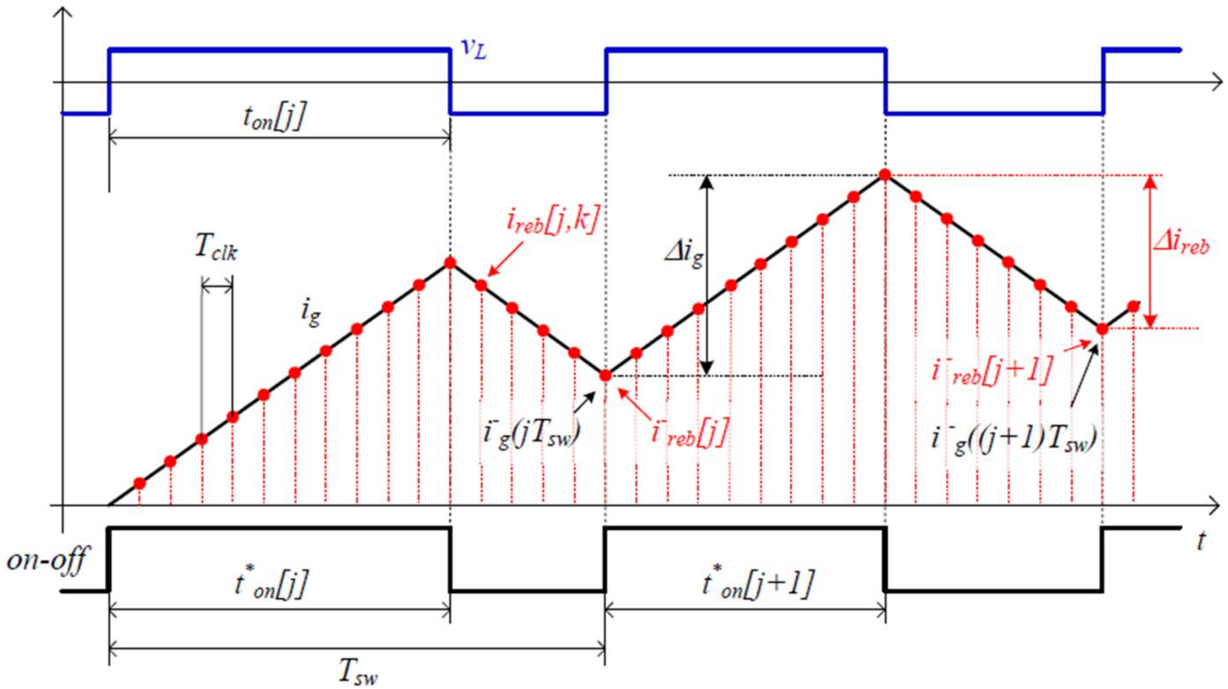
- DCM is also estimated.
- Minimum estimated current forced to zero.
- $Mode_{Dig}$ shows that DCM is estimated.

Simulation of the algorithm (ideal)



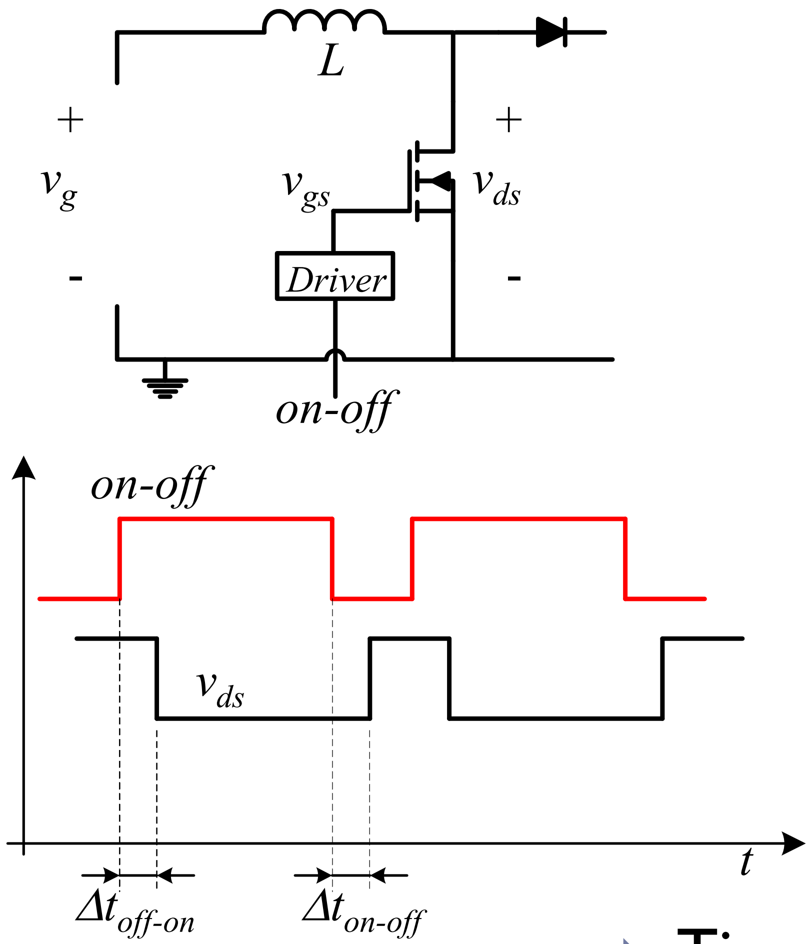
- Left with DCM. Right always in CCM.
- Algorithm not modified for DCM.
- ModelSim simulation (*student edition*).

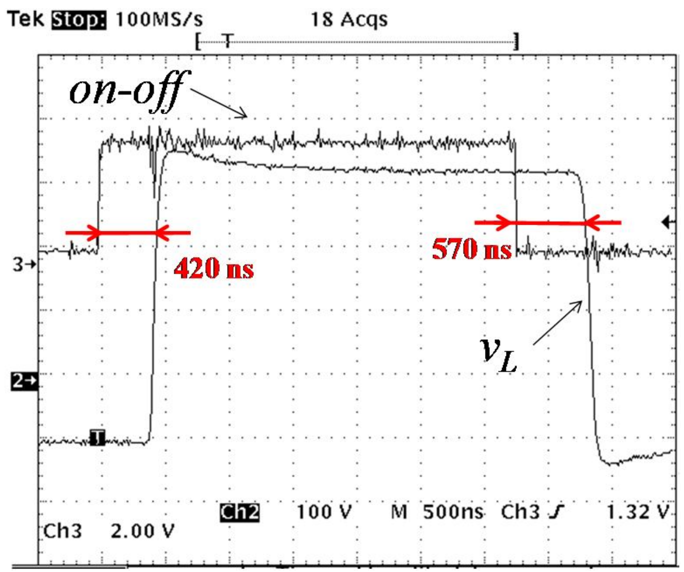
Estimation errors



- Ideal case

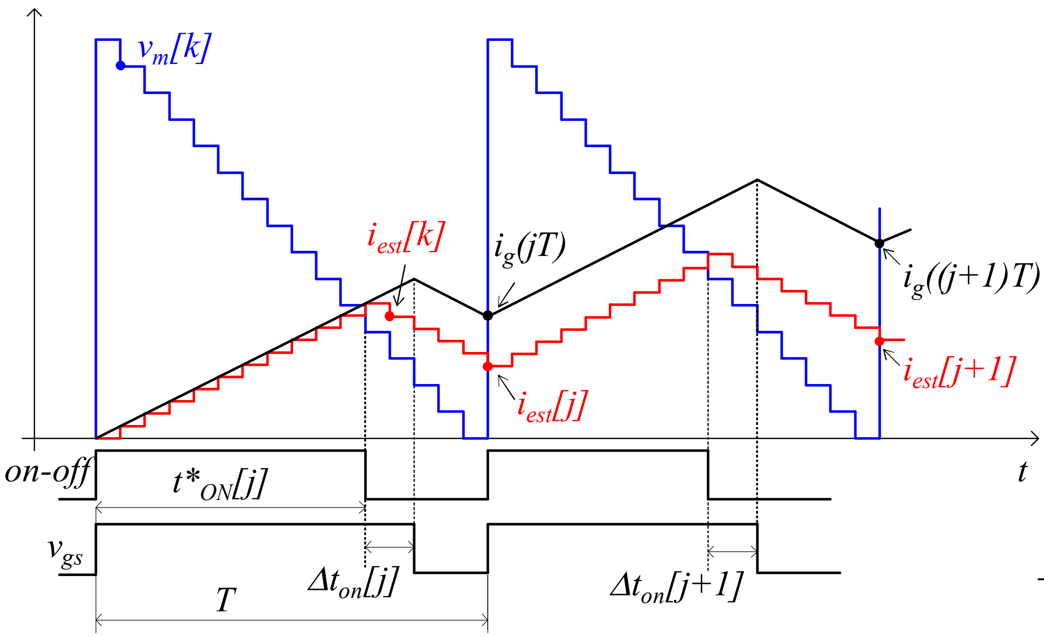
Estimation errors

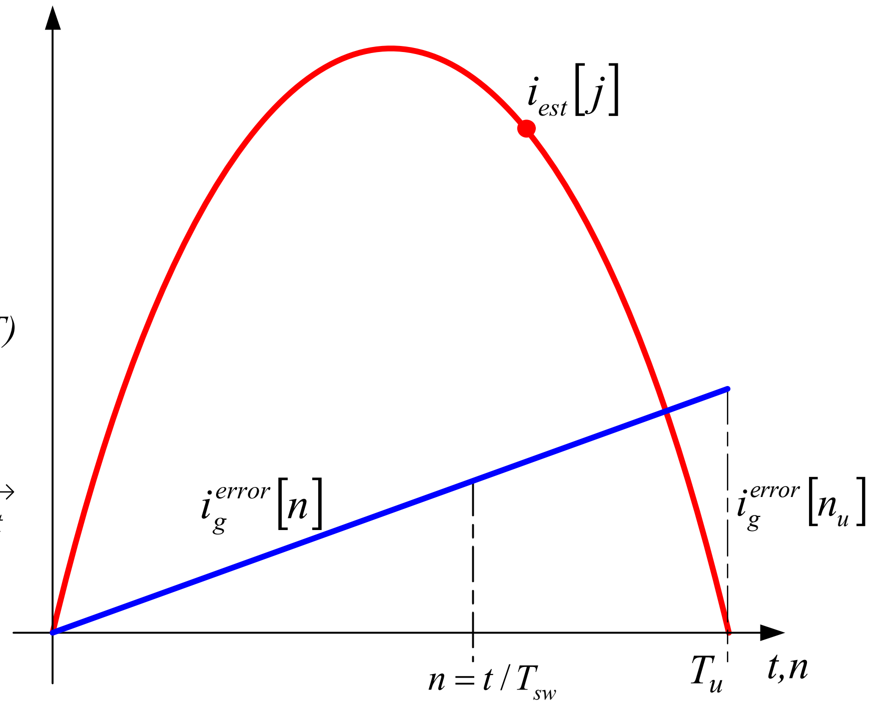




- Time error

Estimation errors



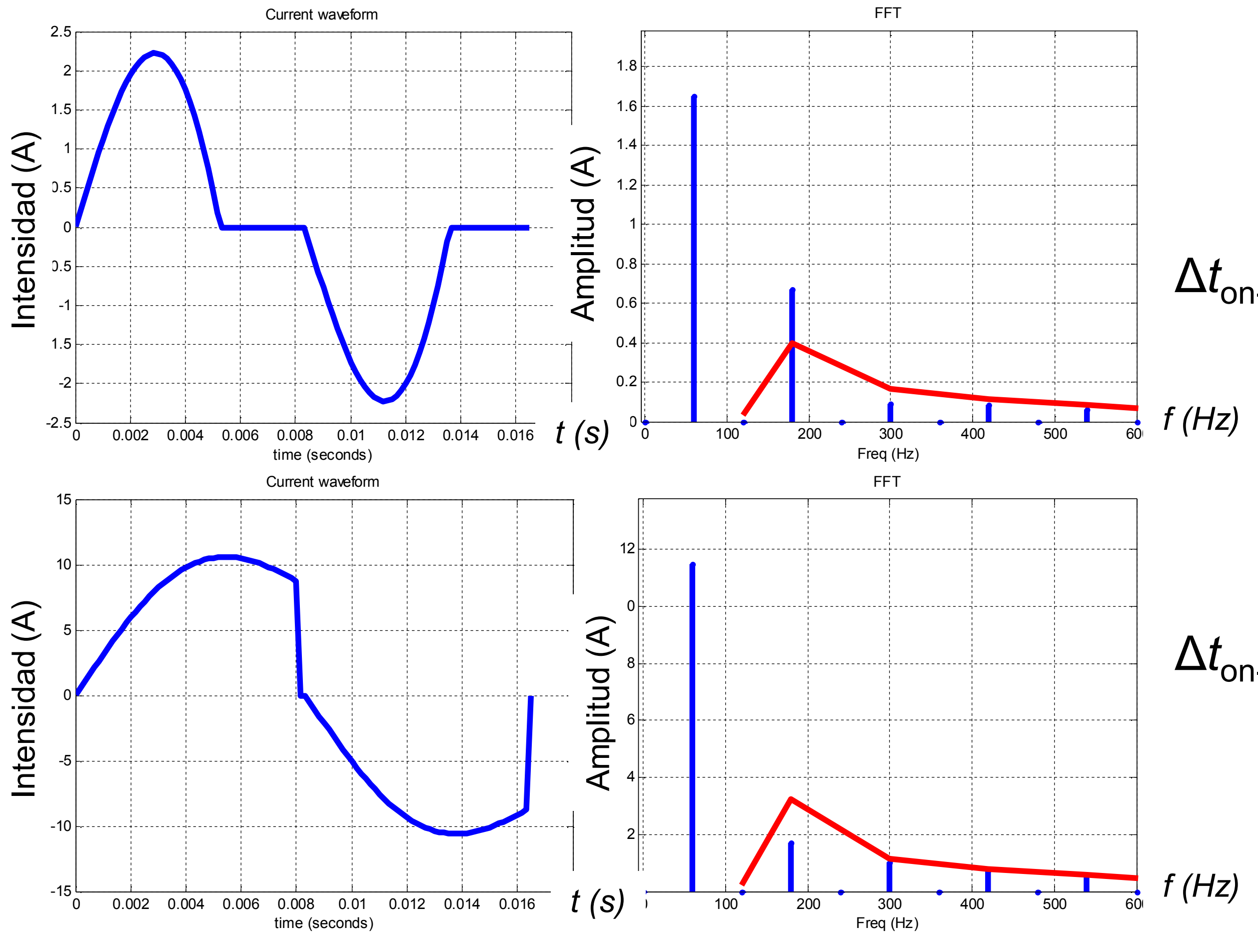


$$\Delta t_{ON}[j] = t_{ON}[j] - t^*_{ON}[j] = \Delta t_{on-off} - \Delta t_{off-on}$$

$$i_g^{error}[n] = \sum_{j=1}^{j=n} \frac{v_o[j]}{L} \Delta t_{ON}[j] \cong \frac{V_o}{L} \frac{\Delta t_{on}}{T} t$$

- Accumulation of the time error

Estimation errors

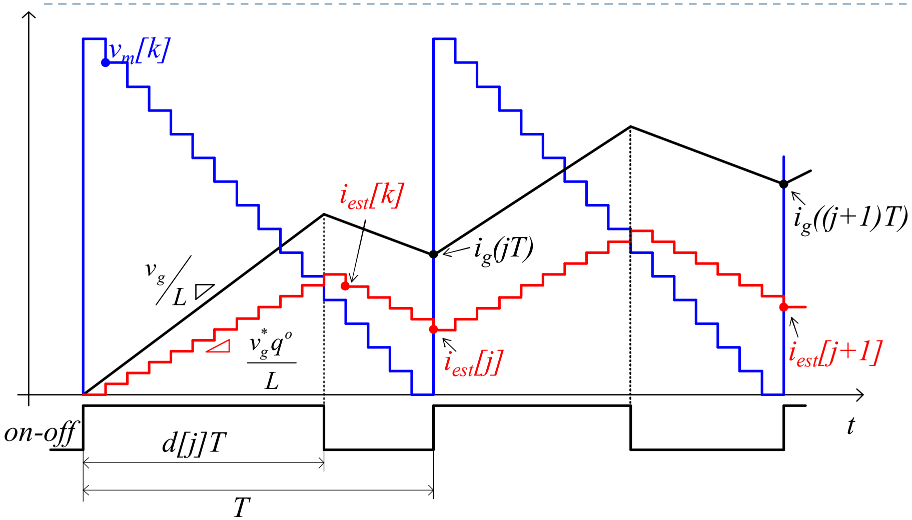


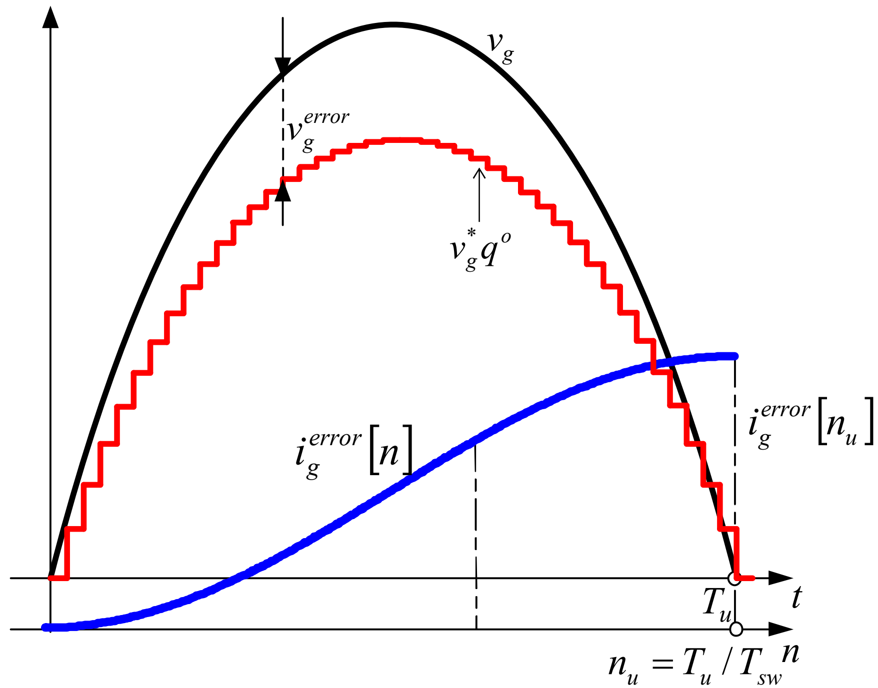
$\Delta t_{\text{on-off}}$ = 40 ns, $\Delta t_{\text{off-on}}$ = 80 ns

$\Delta t_{\text{on-off}}$ = 80 ns, $\Delta t_{\text{off-on}}$ = 40 ns

- Effect of the time error

Estimation errors





	± 1 LSB	
Nbits	$i_g^{error}[n_u]$	q^o(V/bit)
10	± 2.94 A	0.4617
11	± 1.47 A	0.2307
12	± 0.73 A	0.1153
13	± 0.36 A	0.0578

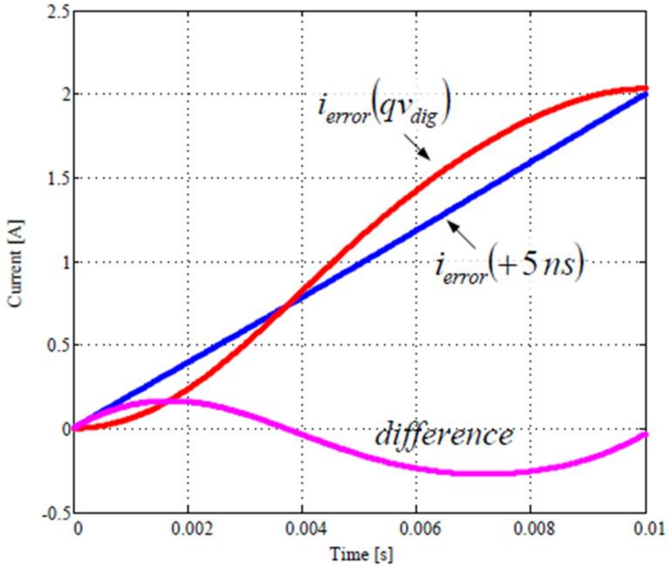
$$i_g^{error}[n] = \sum_{j=1}^{n} \frac{T v_g^{error}[j]}{L}$$

Δt_{on} = 10 ns ➔ $i_g^{error}[n_u]$ = 2.92 A

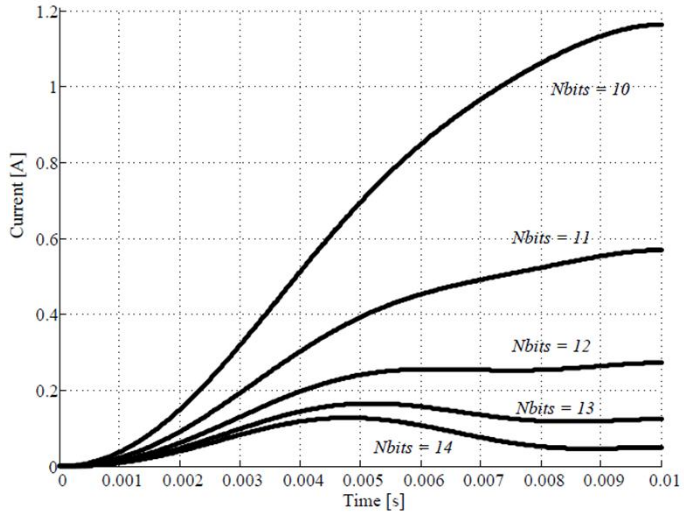
- Effect of the voltage measurement error

Estimation errors

- Comparison of voltage and time resolution



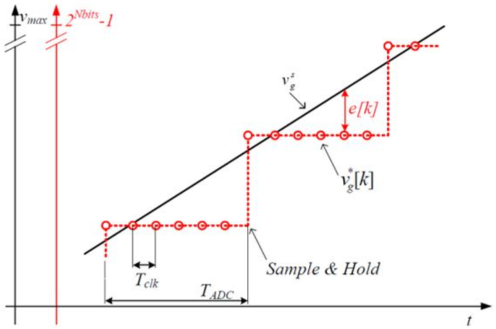
Equivalent current estimation error generated by T_{clk} = 10 ns and due to $Nbits = 10$

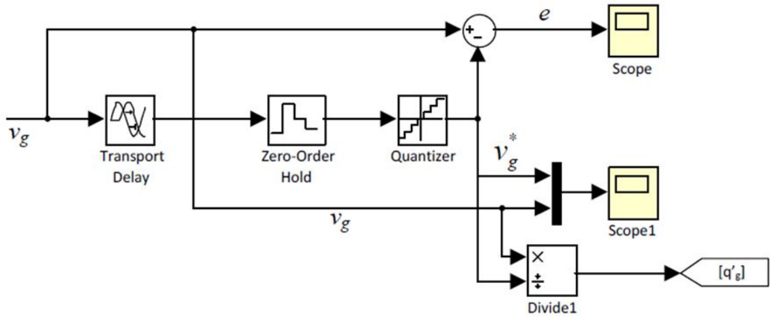


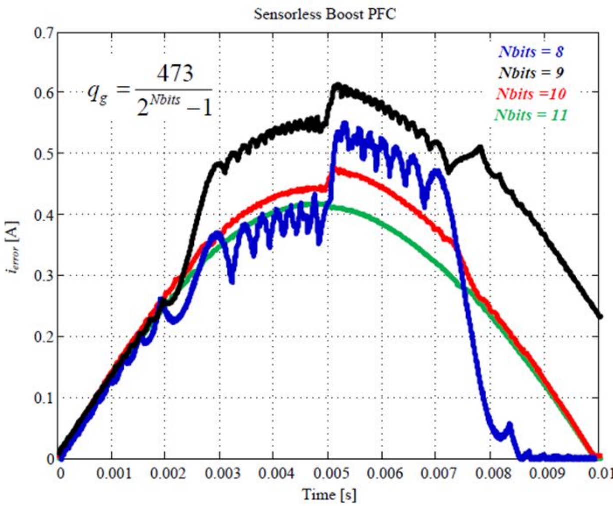
Minimum current estimation error due to the resolution of ± 0.5 *LSB*

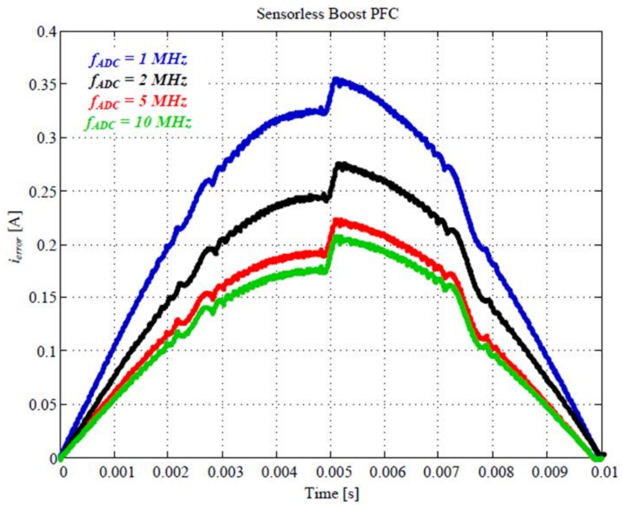
Estimation errors

- Quantization effects



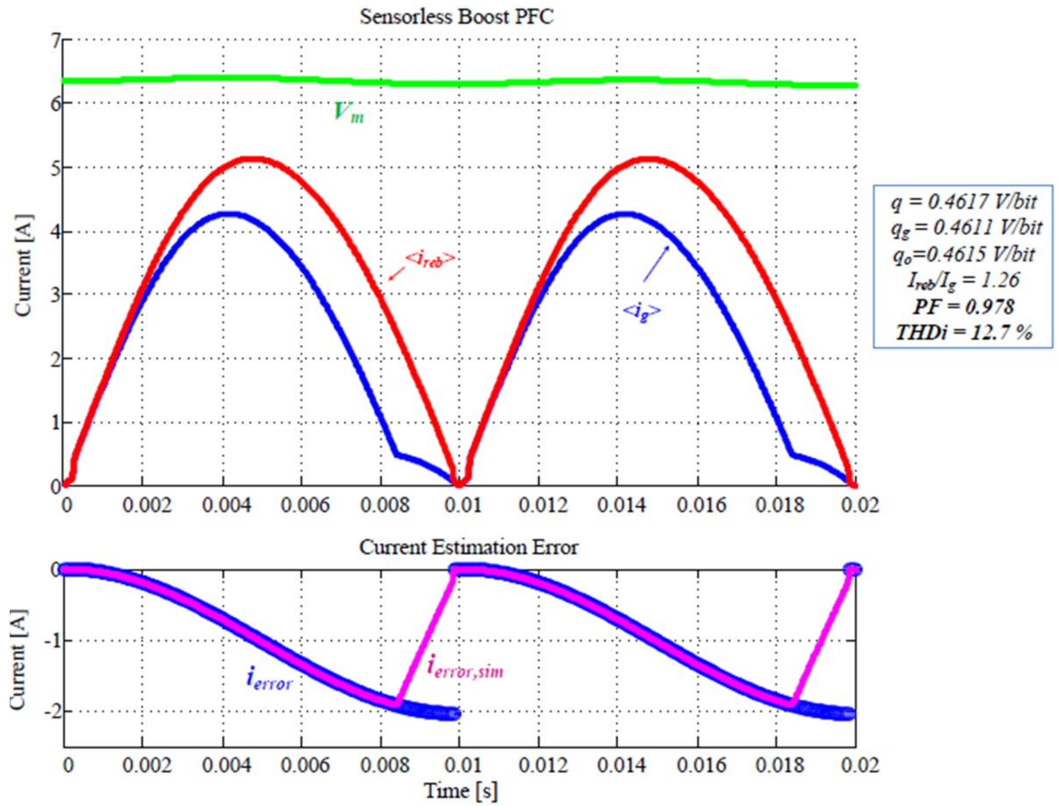




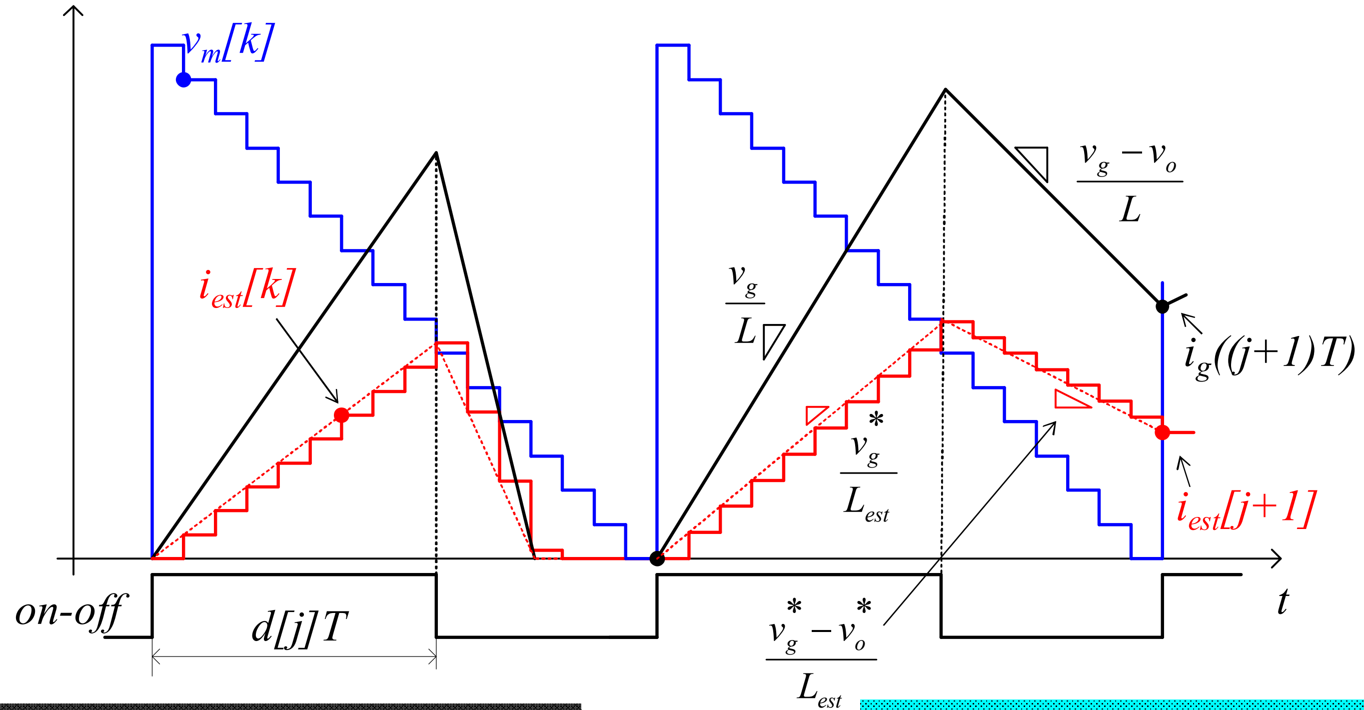


Estimation errors (V)

- Effect of the error in the voltage measurement



Estimation errors



[redacted]

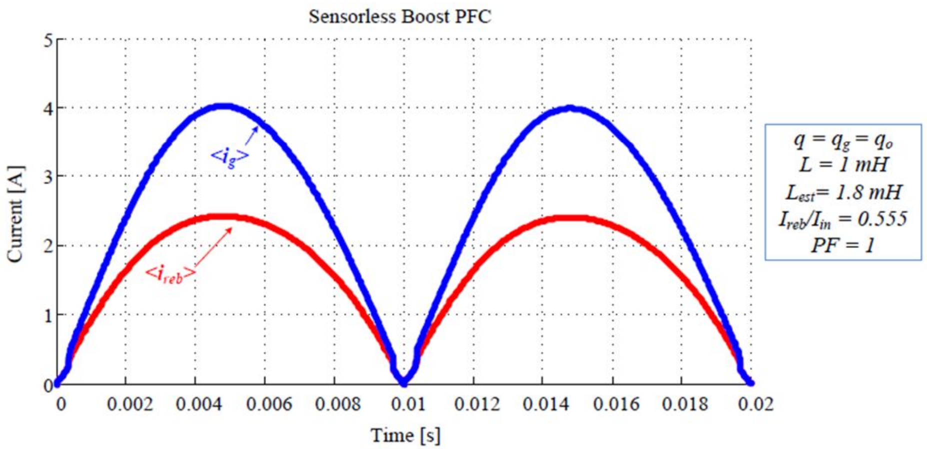
$$i_{est}[j] = \frac{v_g^*}{L_{est}} d[j]T + \frac{v_g^* - v_o^*}{L_{est}} (1 - d[j])T$$

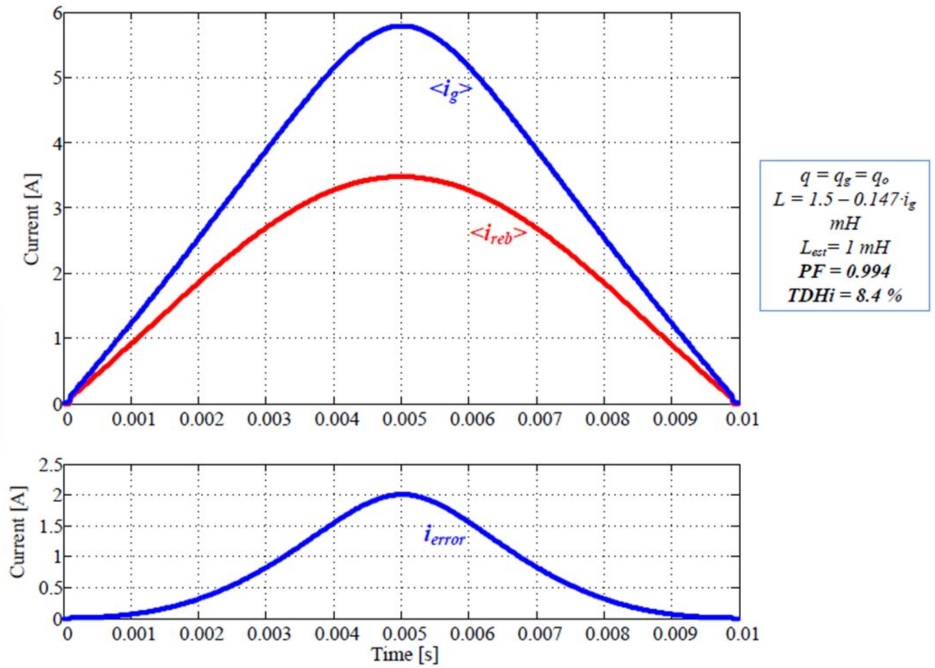
- Error of the inductance value

$$i_g[j] = i_{est}[j] \frac{L_{est}}{L}$$

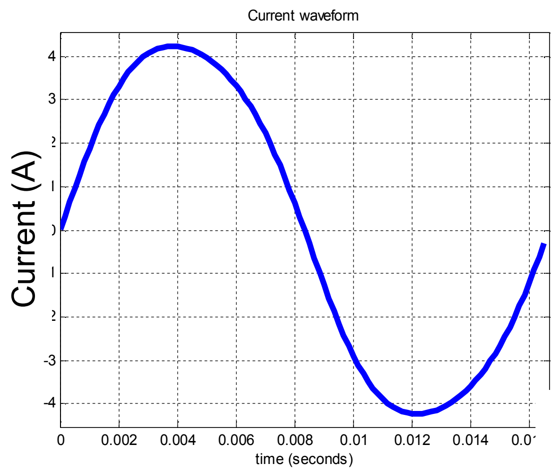
Estimation errors

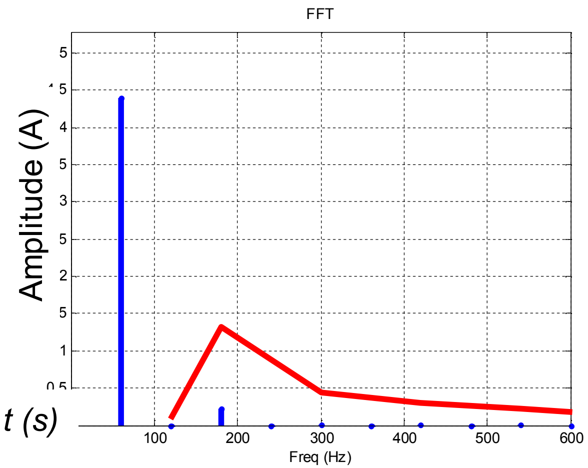
- Error of the inductance value





Contribution of v_o ripple

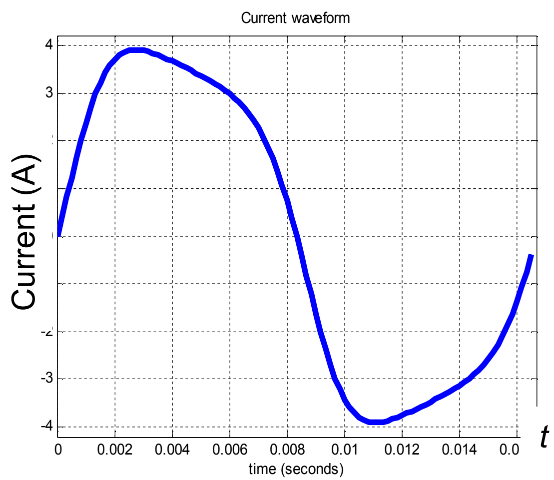


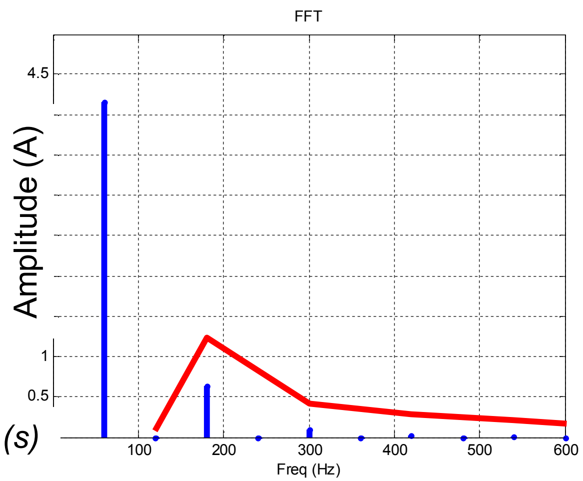


$t\ (s)$ $f\ (Hz)$

$$V_m \frac{V_{gpk}\sin(\omega t)}{V_o - \Delta V_o \sin(2\omega t)} = r_s i_{gpk}$$

$\Delta V_o / V_o = 10\%$



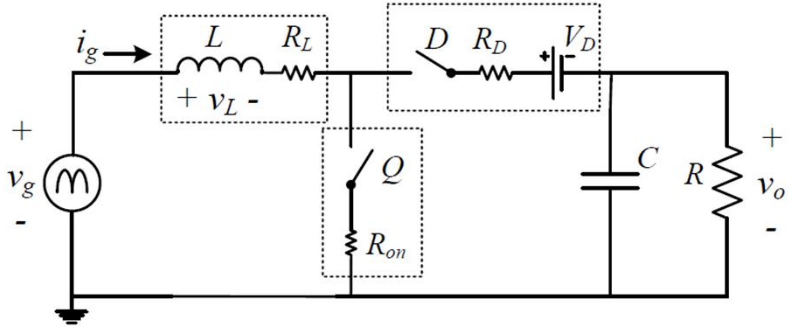


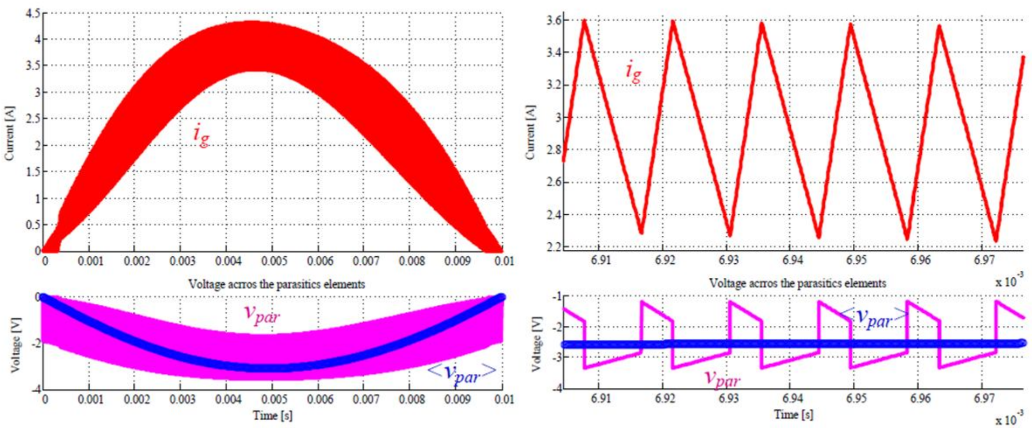
$t\ (s)$ $f\ (Hz)$

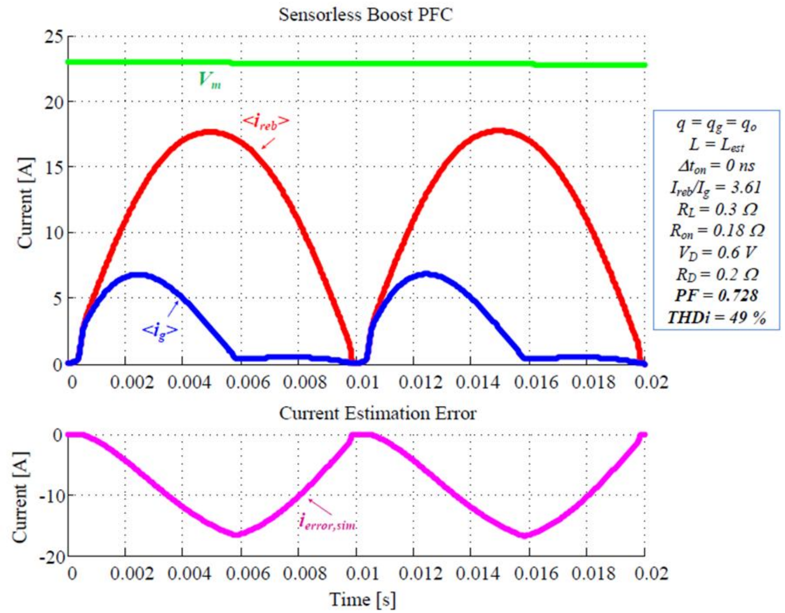
$\Delta V_o / V_o = 30\%$

Current observer does not account for Δv_o

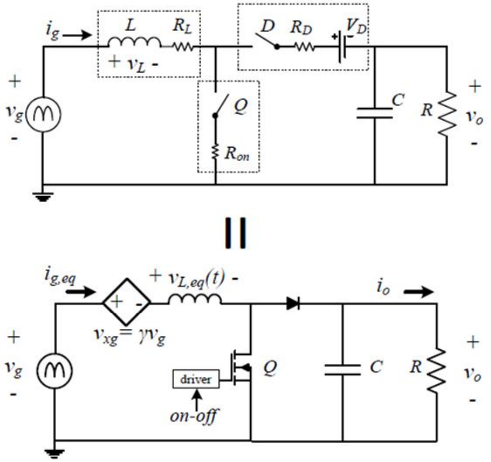
Parasitic elements

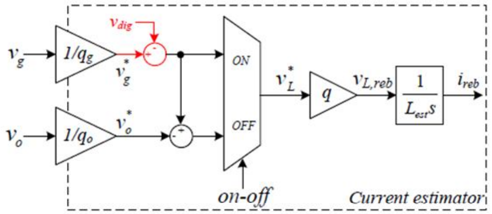




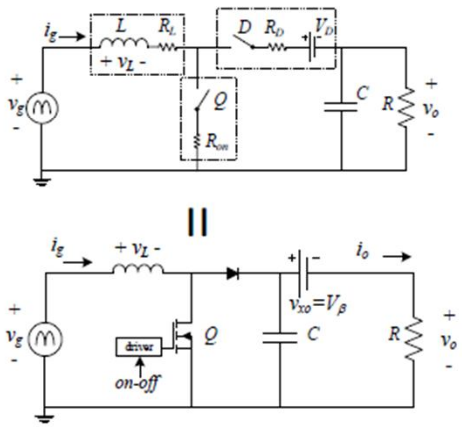


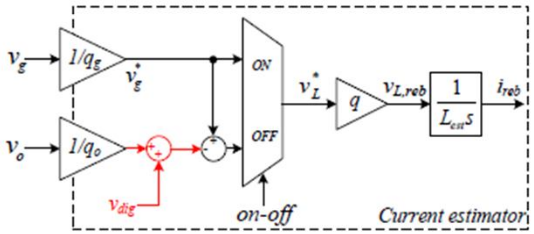
Parasitic elements

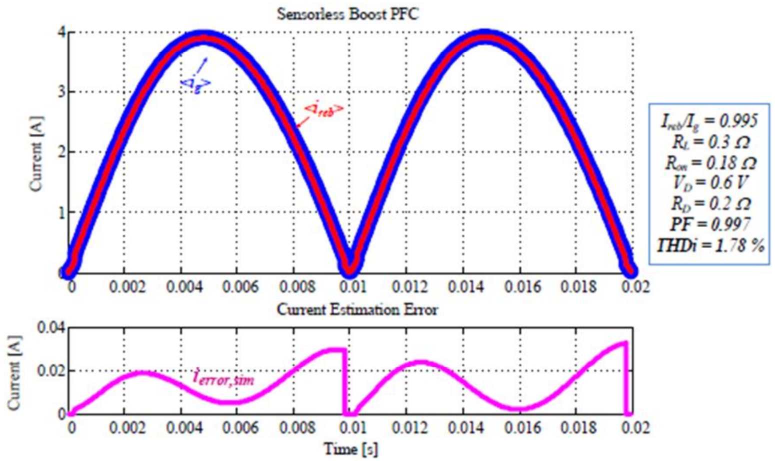




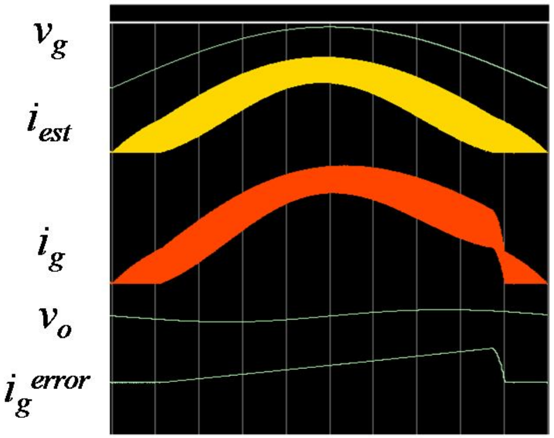
$$qv_{dig} = V_{\beta}$$

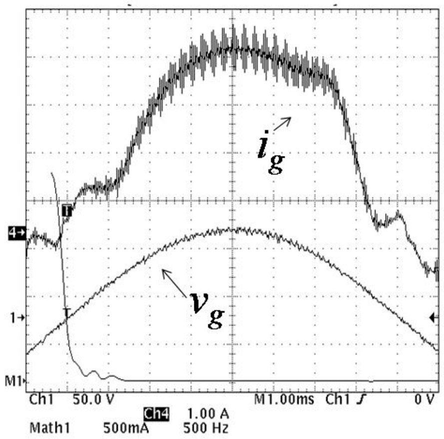


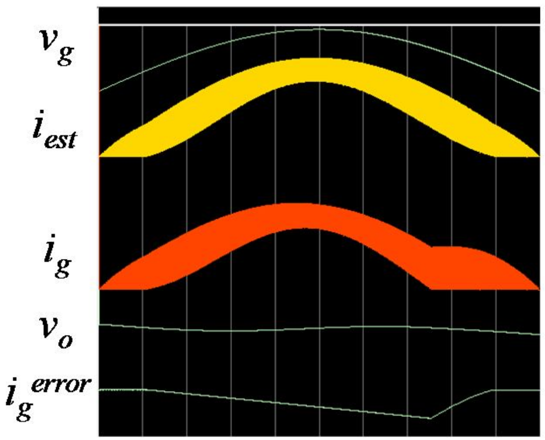


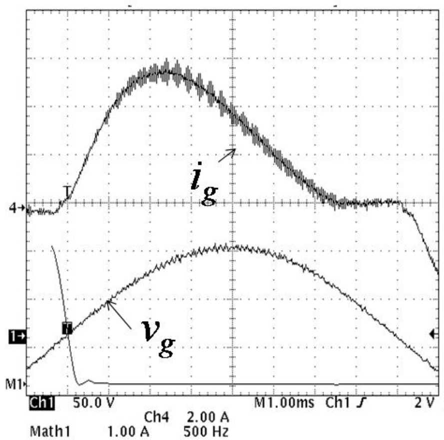


Summary of the effect of the errors









- $V \cdot s$ error

Estimated $V{\cdot}s$ < actual $V{\cdot}s$ across the inductor

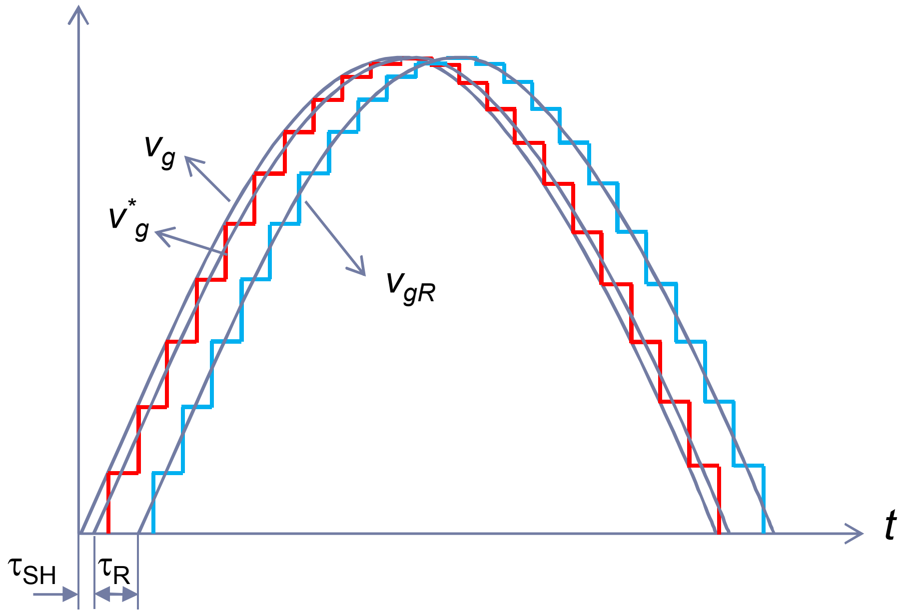
Estimated $V{\cdot}s$ > actual $V{\cdot}s$ across the inductor

Error compensation

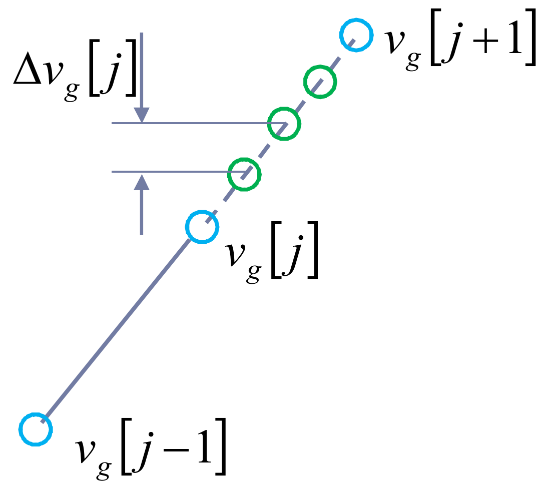
- *Feedforward and feedback*

Error compensation

- Extrapolation

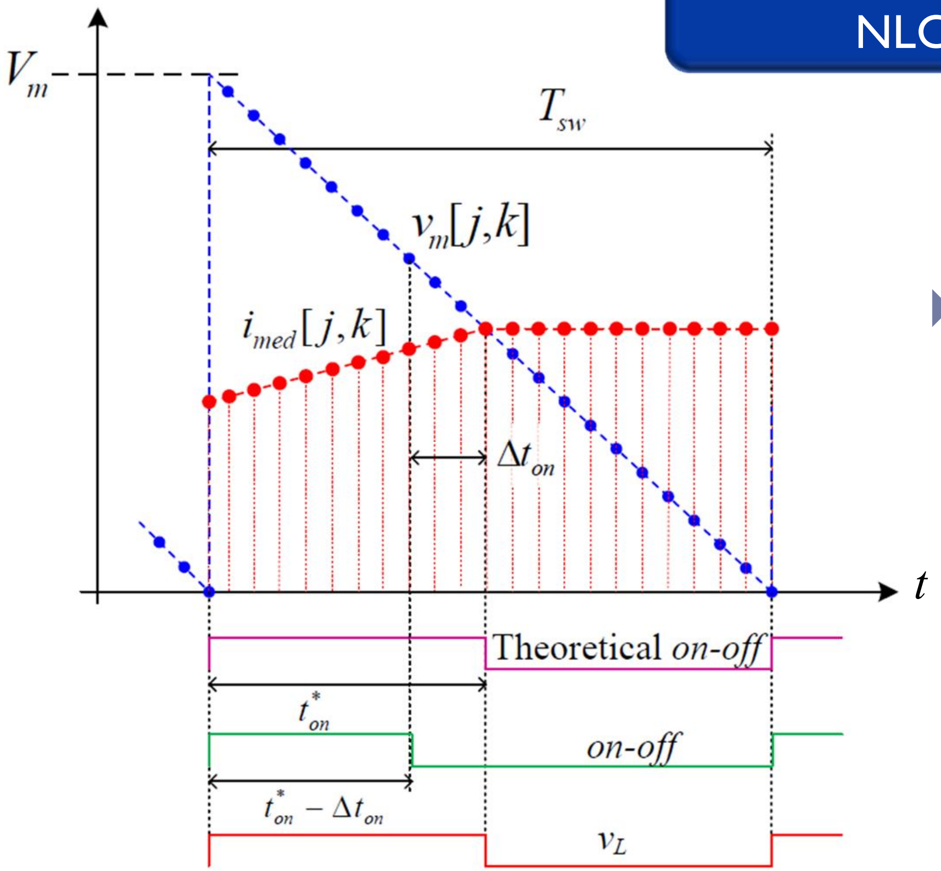


$$\Delta v_g[j] = \frac{v_g[j] - v_g[j-1] f_{ADCclk}}{f_{clk}}$$



Error compensation

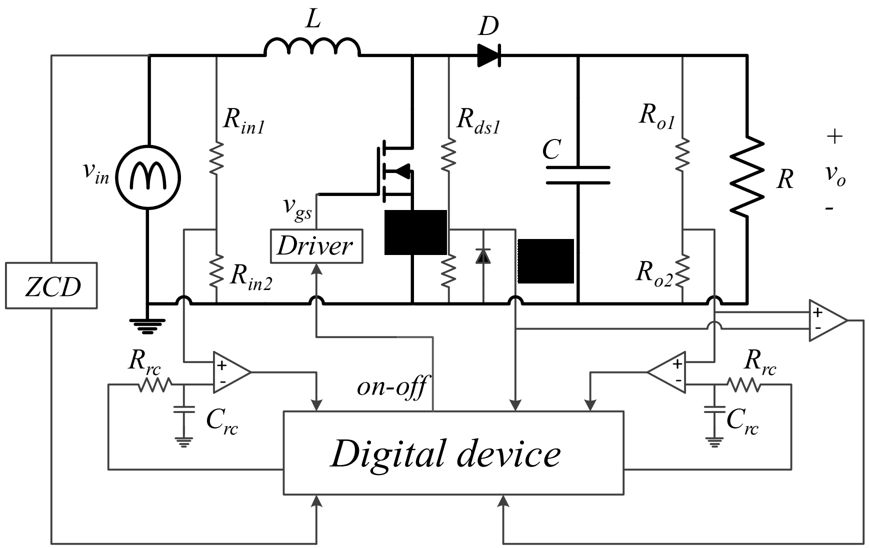
Modification of the NLC

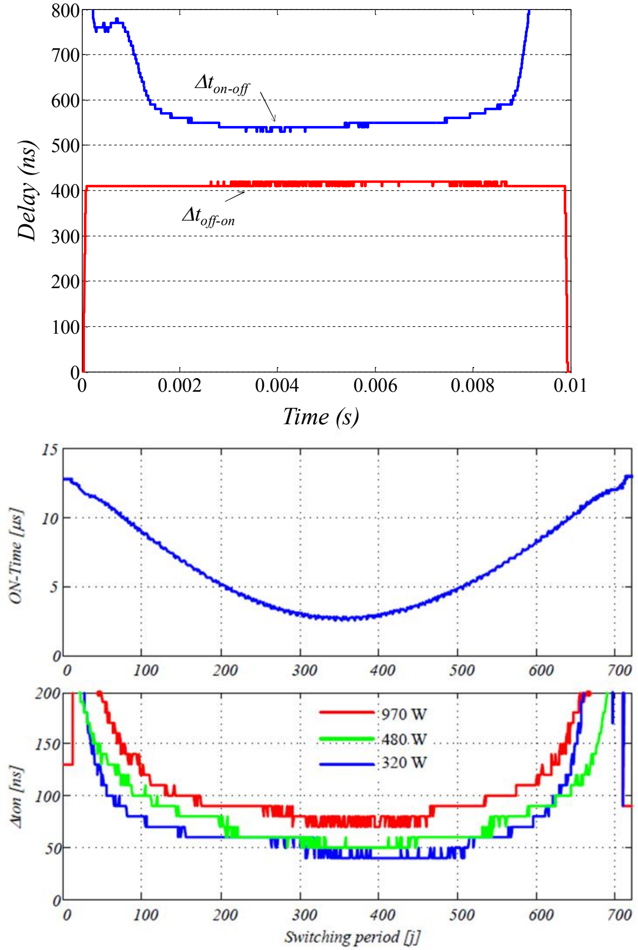


- Ideal case: delay and compensation are coincident

Error compensation

Delay measurement

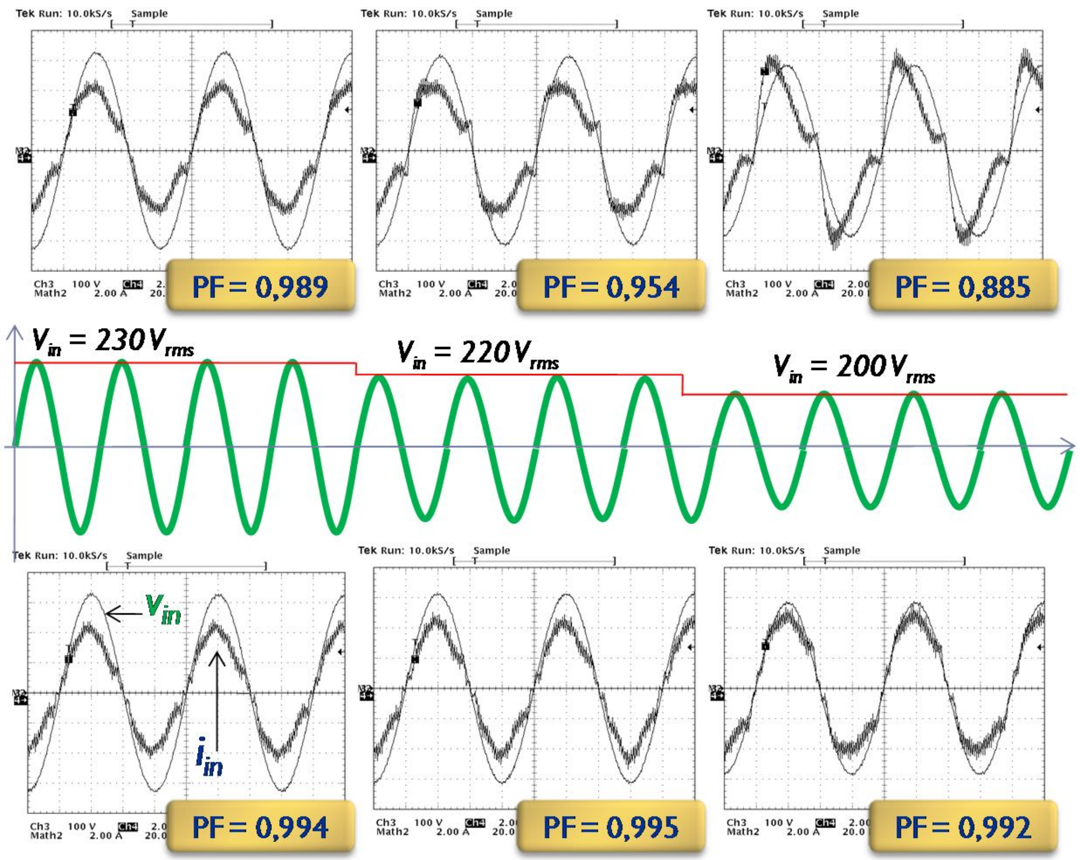




L = 1 mH (3A)
V_o = 400 V
f_s = 73.2 kHz
P_o = 640 W

Error compensation

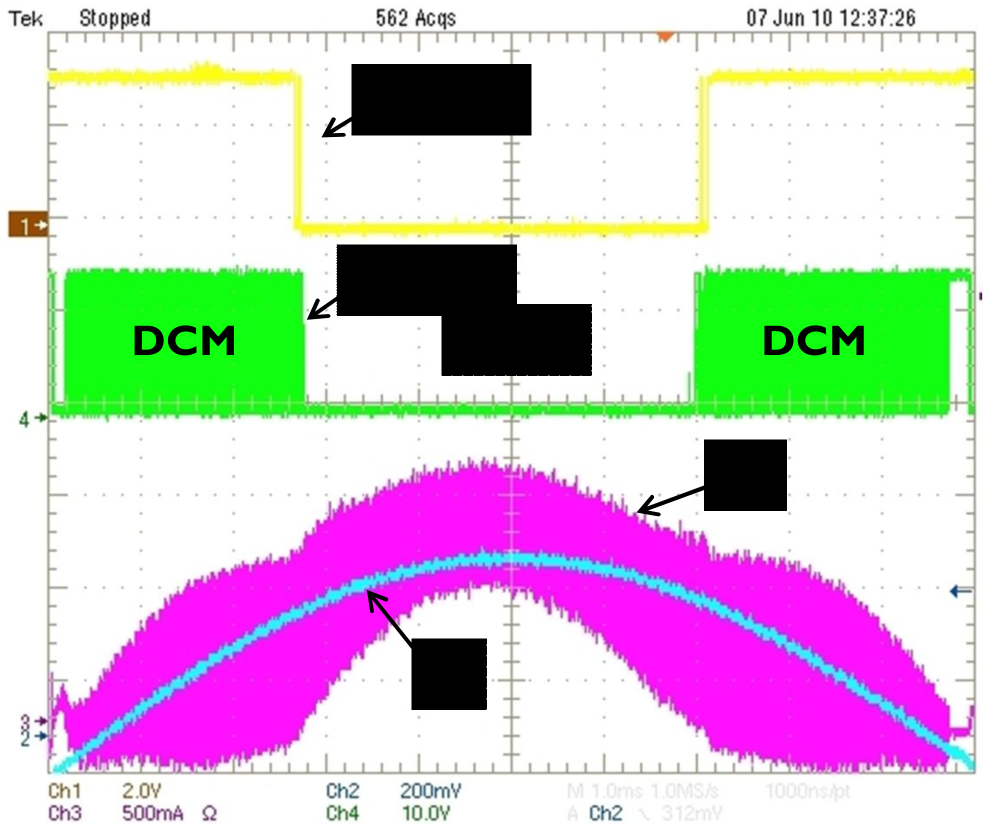
Delay compensation



- Initial
- Continuous

Feedback compensation

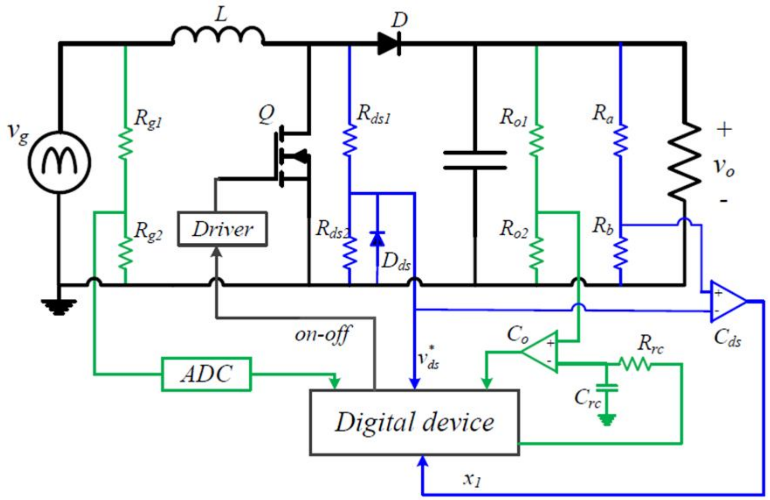
$f_s = 73.2\ kHz$
$P_o = 160\ W$
$V_g = 230\ V_{rms}$ (50 Hz)

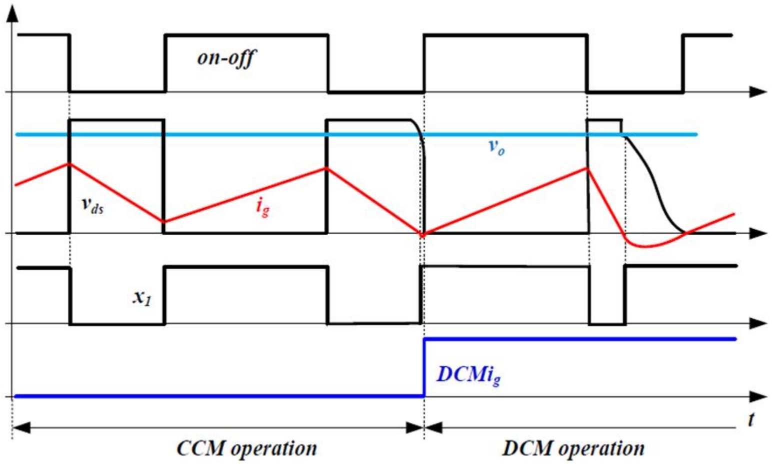


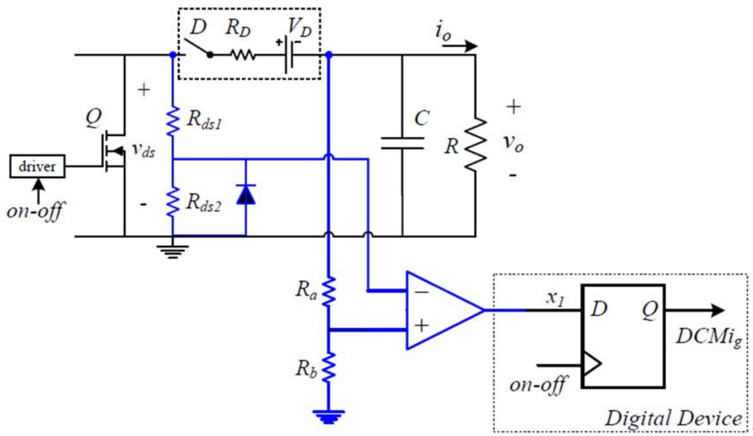
- $Mode_{Dig}$= “1” if the algorithm calculates $i_{in} \leq 0$.
- $Mode_{Real}$= “1” if DCM is reached during the switching period.

Feedback compensation

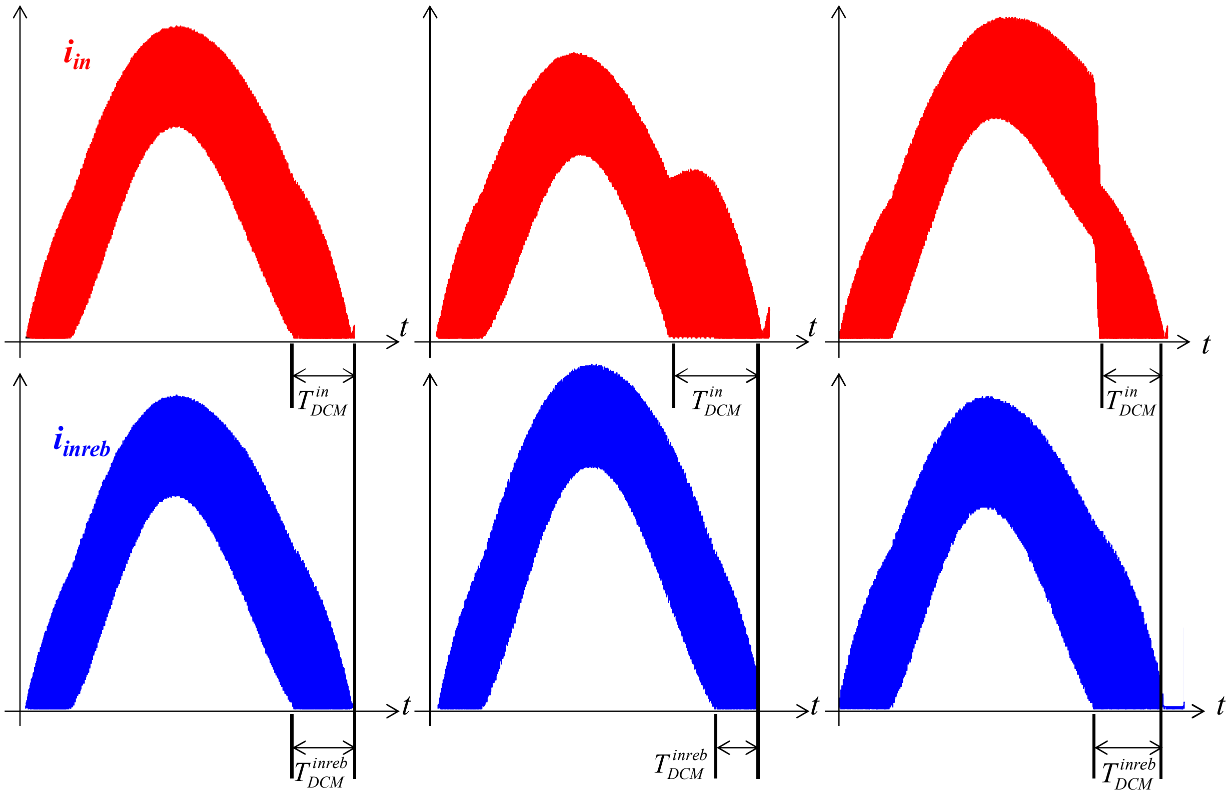
DCM detection







Feedback compensation



Δt_{on}=0 ns

$T^{in}_{DCM} = T^{inreb}_{DCM}$

Δt_{on}=-10 ns

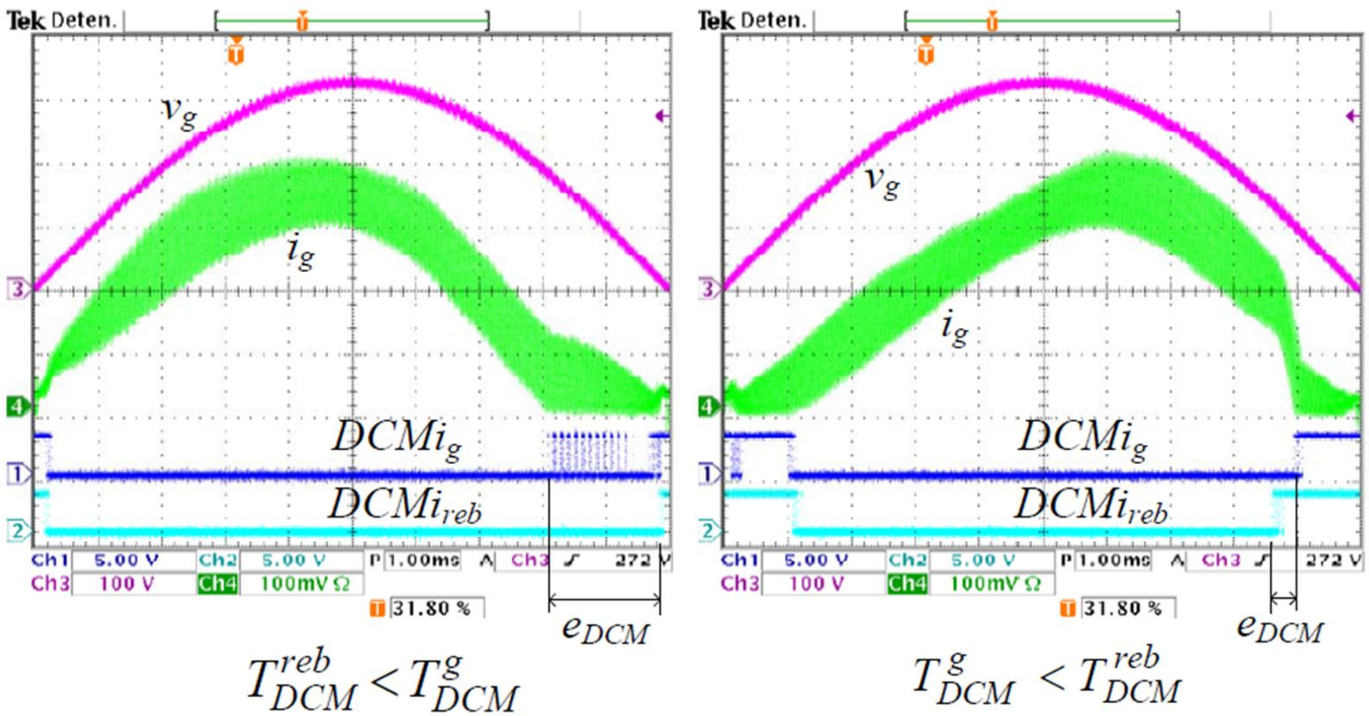
$T^{in}_{DCM} > T^{inreb}_{DCM}$

Δt_{on}=10 ns

$T^{in}_{DCM} < T^{inreb}_{DCM}$

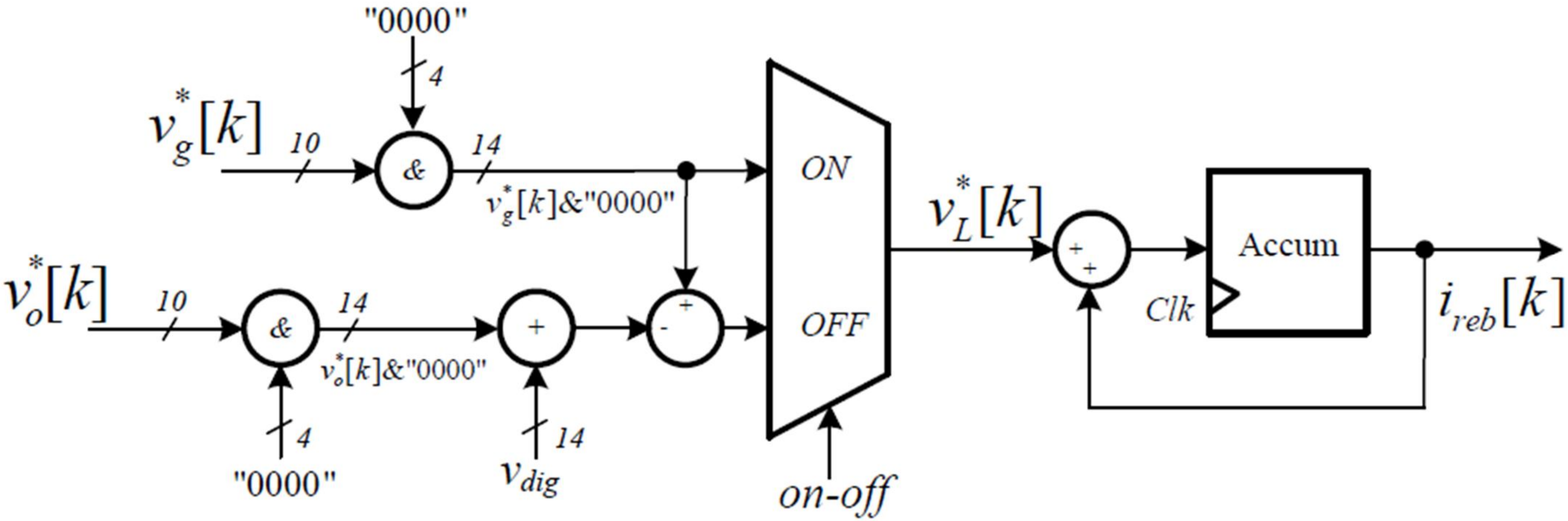
$$e_{DCM} = T^{in}_{DCM} - T^{inreb}_{DCM}$$

Feedback compensation

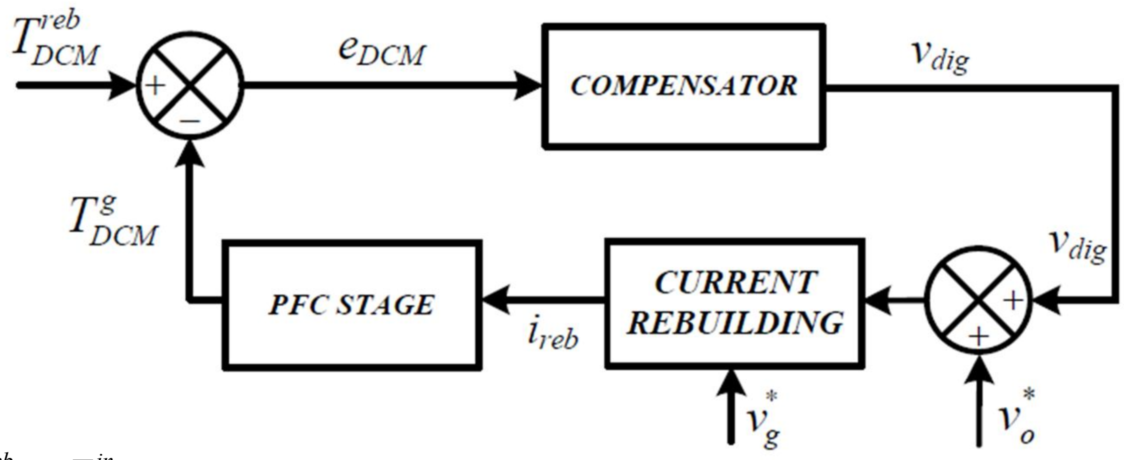


$$e_{DCM} = T_{DCM}^{in} - T_{DCM}^{inreb}$$

Feedback compensation



Feedback compensation



$$e_{DCM} = T_{DCM}^{reb} - T_{DCM}^{in}$$

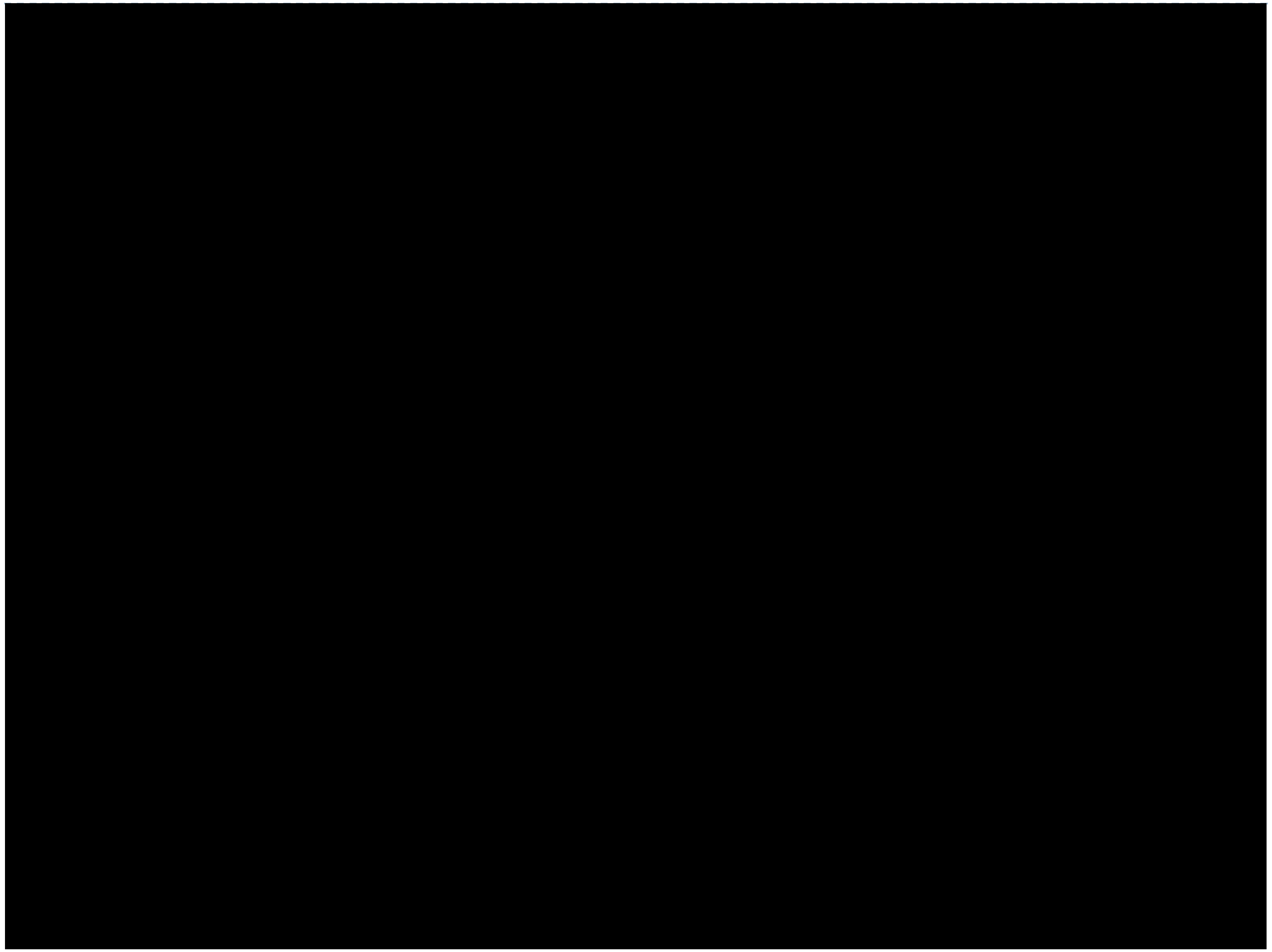
Plant to control $G_{Tv} = \dfrac{\partial T_{DCM}^{g}}{\partial v_{dig}} \cong -\dfrac{q}{\Gamma}$ around the operation point $qV_{dig} = V_{\beta}$

$$\Gamma = \frac{V_o \pi^2 f_u^2 L}{R}\left(\frac{2}{M_g^2} + \frac{D_{\max}}{K}\right) \qquad I_g = \frac{V_o^2}{RV_g}$$

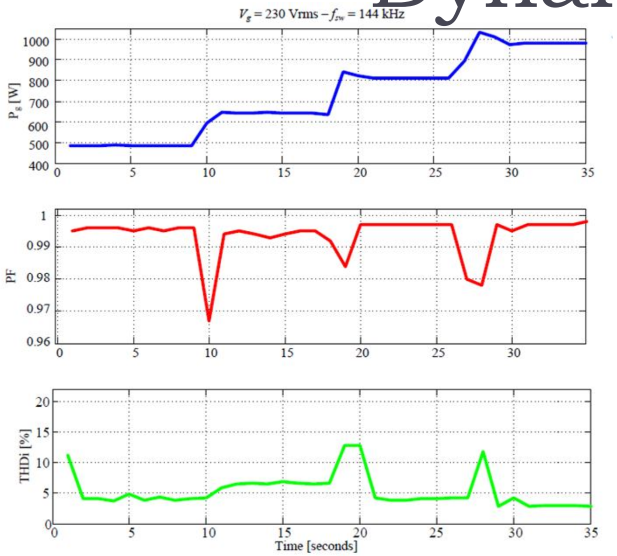
$$M_g = \frac{V_{g,peak}}{V_o} \qquad K = \frac{2Lf_{sw}}{R}$$

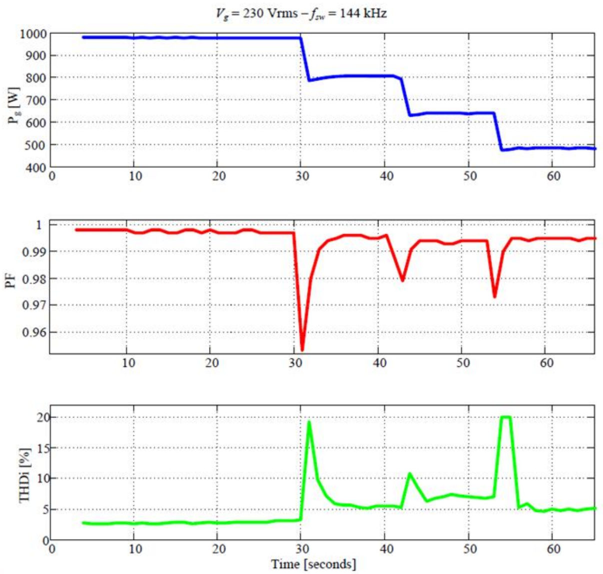
V. M. Lopez-Martin, F. J. Azcondo, A. de Castro, "Modeling of a High resolution DCM times feedback loop for Sensorless Boost PFC stages," in Proc. Control and Modeling for Power Electronics (COMPEL), 2013

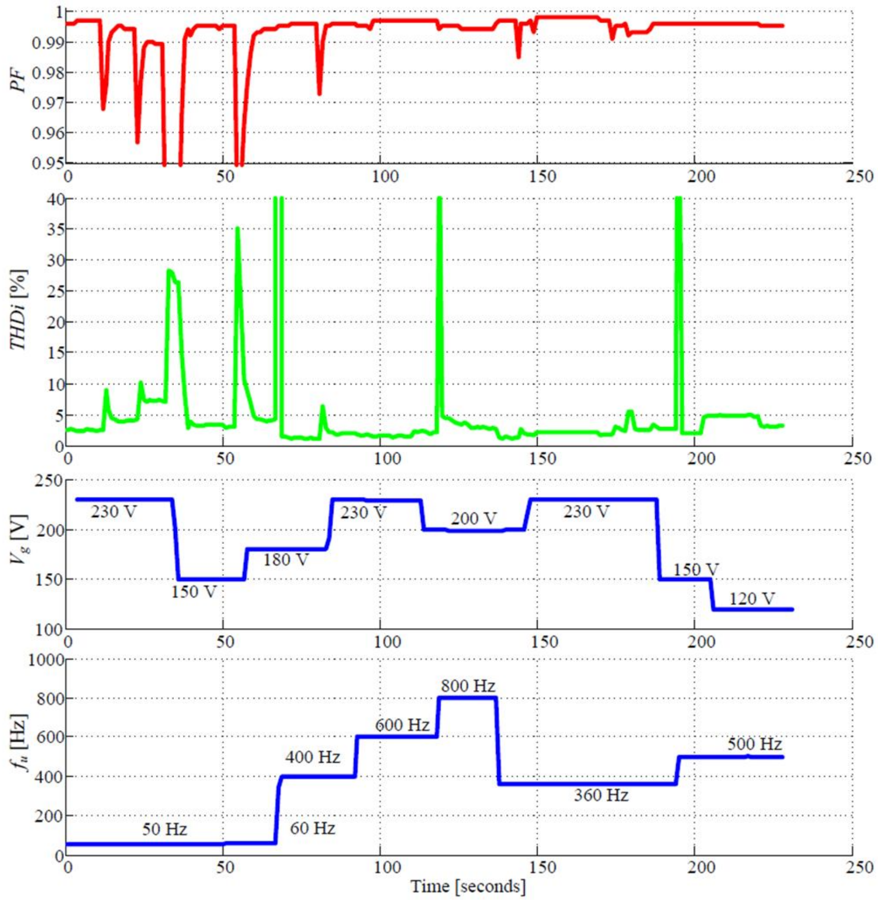
Operation as a resistor emulator



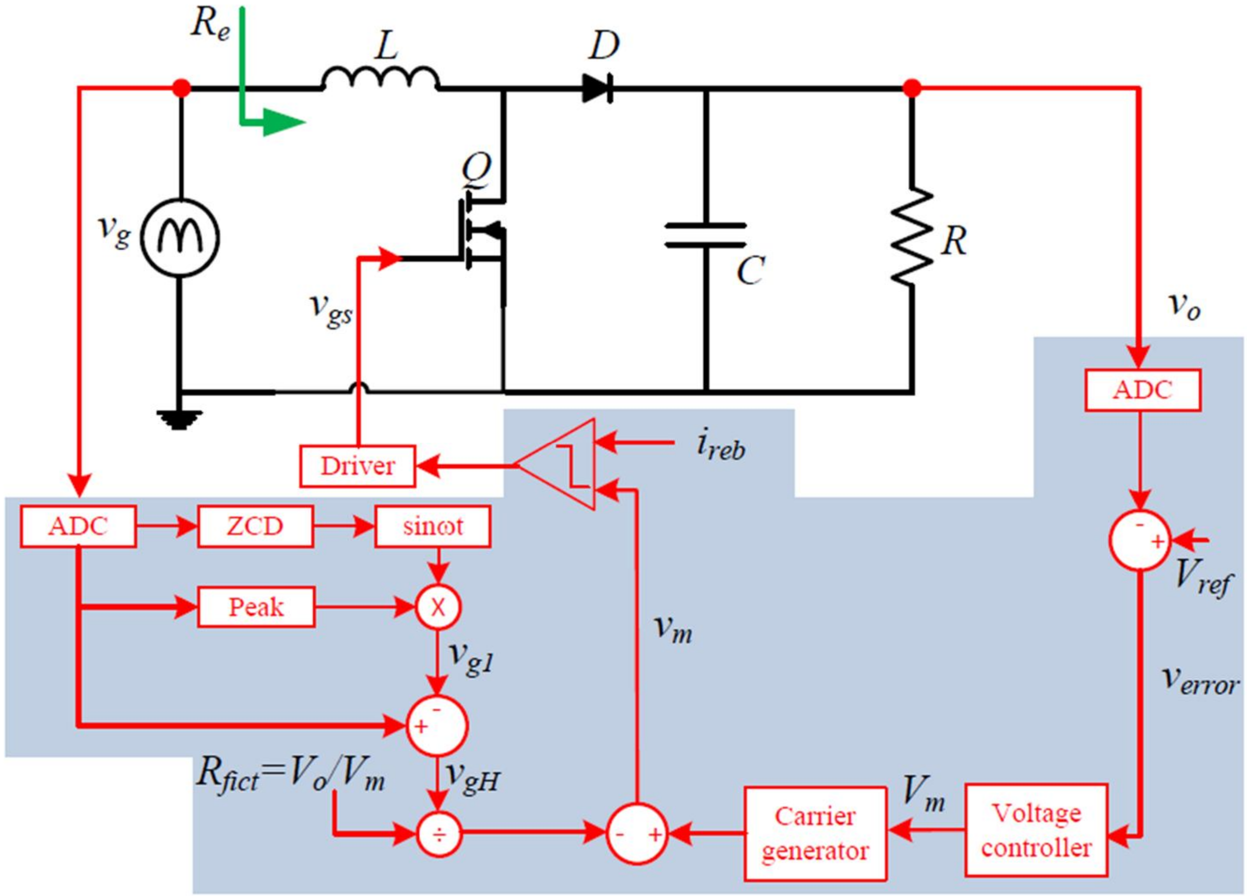
Dynamic response





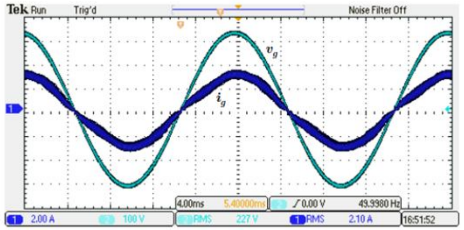


Low THDi

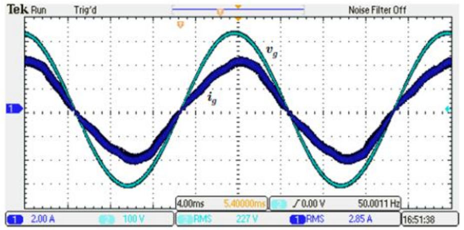


R_e
L
D
Q
v_g
v_{gs}
C
R
v_o
ADC
i_{reb}
Driver
ADC
ZCD
sinωt
Peak
X
v_{g1}
V_{ref}
v_m
v_{error}
$R_{fict}=V_o/V_m$
v_{gH}
÷
V_m
Carrier generator
Voltage controller

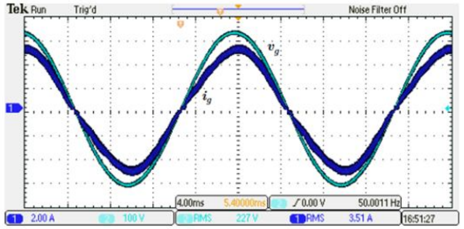
Experimental results



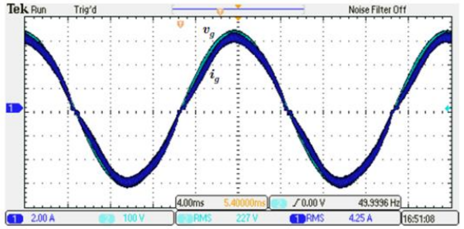
(a) P_g =483.1 W, PF =0.994, $THDi$ =6.20 %



(b) P_g =640.6 W, PF =0.994, $THDi$ =6.93 %

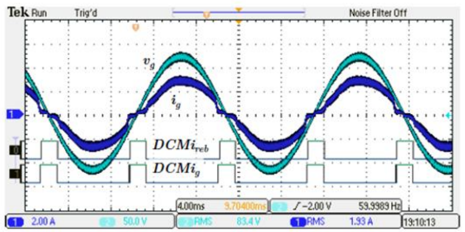


(c) P_g =807.2 W, PF =0.995, $THDi$ =5.48 %

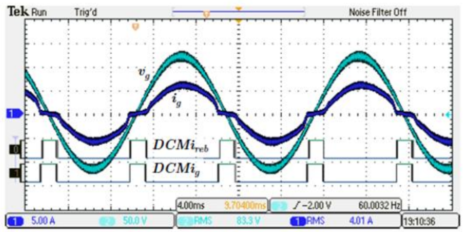


(d) P_g =978.8 W, PF =0.998, $THDi$ =2.78 %

V_o = 400 V_{dc}, L_1 = 1mH (R_{L1} = 0.25 Ω)
V_g = 230 V_{rms}(50Hz)



(a) P_g =167.4 W, PF =0.991, $THDi$ =7.83 %



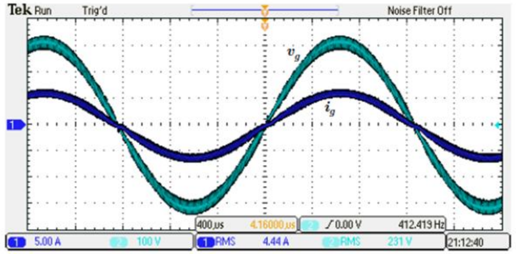
(b) P_g =346.6 W, PF =0.988, $THDi$ =11.13 %

V_o = 400 V_{dc}, L_1 = 1mH (R_{L1} = 0.25 Ω)
V_g = 85 V_{rms}(60Hz)

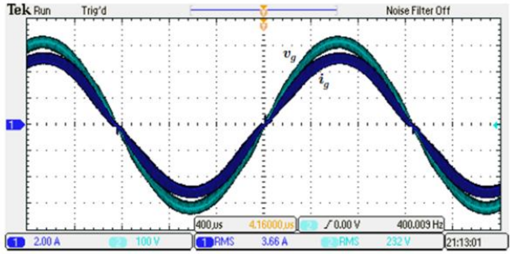
				Current Harmonics (A)						
V_g	P_g	PF	$THDi$	I_1	I_2	I_3	I_5	I_7	I_9	I_{11}
250 V	480.5 W	0.992	7.57 %	1.932	0.008	0.130	0.031	0.024	0.008	0.014
				Limits	0.039	0.575	0.193	0.135	0.097	0.058
	638.8 W	0.994	6.99 %	2.582	0.011	0.174	0.037	0.033	0.013	0.018
				Limits	0.052	0.770	0.258	0.181	0.129	0.077
	806.7 W	0.997	5.55 %	3.241	0.008	0.177	0.012	0.016	0.007	0.014
				Limits	0.065	0.969	0.324	0.227	0.162	0.097
	978.4 W	0.999	3.07 %	3.888	0.018	0.086	0.057	0.028	0.023	0.012
				Limits	0.078	1.165	0.389	0.272	0.194	0.117
230 V	483.1 W	0.994	6.20 %	2.117	0.003	0.119	0.048	0.026	0.014	0.018
				Limits	0.042	0.632	0.212	0.148	0.106	0.064
	640.6 W	0.994	6.93 %	2.805	0.005	0.189	0.031	0.023	0.020	0.021
				Limits	0.056	0.836	0.281	0.196	0.140	0.084
	807.2 W	0.995	5.48 %	3.544	0.005	0.192	0.018	0.022	0.011	0.008
				Limits	0.071	1.058	0.354	0.248	0.177	0.106
	978.8 W	0.998	2.78 %	4.294	0.004	0.056	0.096	0.038	0.017	0.015
				Limits	0.086	1.285	0.429	0.301	0.215	0.129
180 V	487.5 W	0.993	6.53 %	2.713	0.009	0.144	0.055	0.034	0.010	0.024
				Limits	0.054	0.808	0.271	0.190	0.136	0.081
	648.4 W	0.994	4.91 %	3.620	0.005	0.162	0.062	0.035	0.021	0.018
				Limits	0.072	1.080	0.362	0.253	0.181	0.109
	821.8 W	0.996	3.50 %	4.584	0.004	0.035	0.150	0.044	0.038	0.042
				Limits	0.092	1.370	0.458	0.321	0.229	0.138
120 V	331.5 W	0.992	6.61 %	2.776	0.005	0.166	0.056	0.061	0.042	0.038
				Limits	0.056	0.826	0.278	0.194	0.139	0.083
	503.9 W	0.995	5.18 %	4.223	0.004	0.131	0.142	0.104	0.097	0.081
				Limits	0.084	1.260	0.422	0.296	0.211	0.127
85 V	167.4 W	0.991	7.83 %	1.978	0.004	0.084	0.113	0.063	0.051	0.031
				Limits	0.040	0.588	0.198	0.138	0.099	0.059
	346.6 W	0.988	11.13 %	4.119	0.019	0.293	0.273	0.209	0.123	0.042
				Limits	0.082	1.221	0.412	0.288	0.206	0.124

f_{sw} = 144 kHz

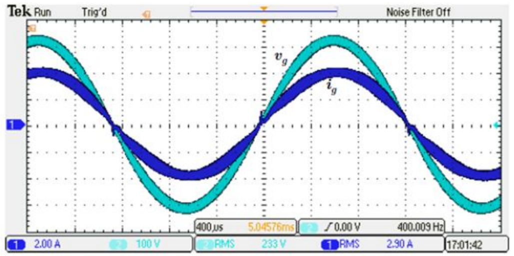
Experimental results



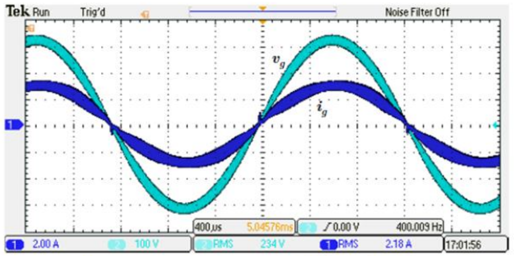
(a) V_g = 224.8 V, f_u = 400 Hz, $THDi$ = 1.49 %, PF = 0.996, P_g = 969.4 W



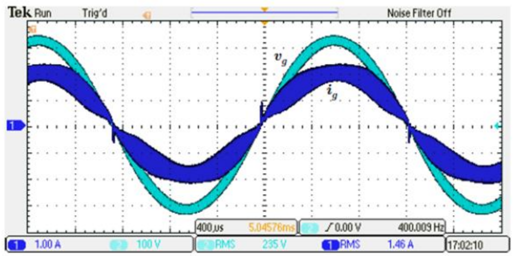
(b) V_g = 225.7 V, f_u = 400 Hz, $THDi$ =1.66 %, PF = 0.995, P_g = 804.2 W



(c) V_g = 226.7 V, f_u = 400Hz, $THDi$ = 2.24 %, PF = 0.992, P_g = 631.5 W



(d) V_g = 225.7 V, f_u = 400 Hz, $THDi$ = 3.52 %, PF = 0.990, P_g = 482.1 W

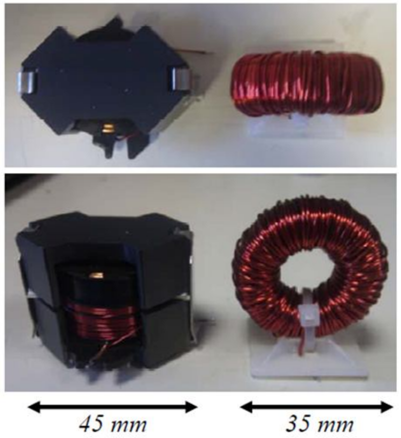


(e) V_g = 225.7 V, f_u = 400 Hz $THDi$ = 4.35 %, PF = 0.982, P_g = 321.3 W

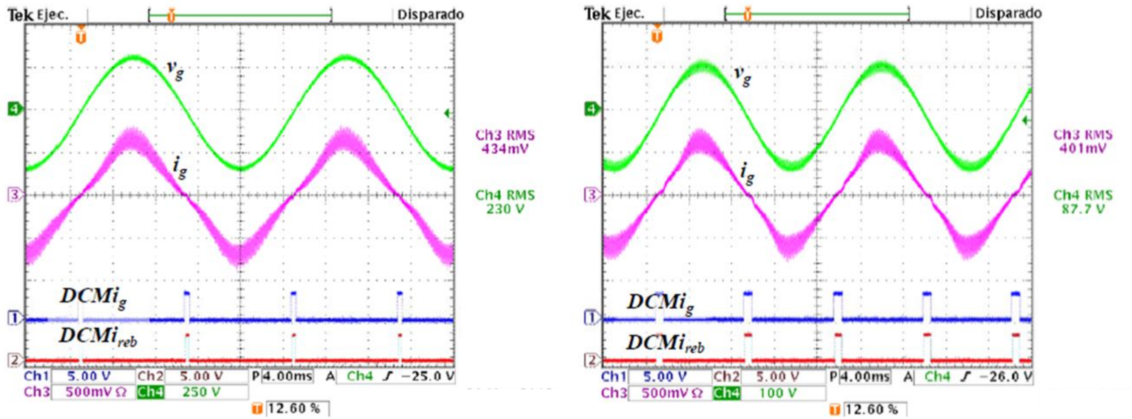
Results at 230 Vrms - 400 Hz sinusoidal grid

V_g (V)	P_g (W)	PF	$THDi$ (%)	I_1 (A)	I_3 (A)	I_5 (A)	I_7 (A)	I_9 (A)	I_{11} (A)
224.8	969.4	0.996	1.49	4.32	0.05	0.02	0.03	0.02	0.02
225.7	804.2	0.995	1.66	3.57	0.05	0.02	0.02	0.02	0.02
226.7	631.5	0.992	2.24	2.72	0.06	0.03	0.02	0.01	0.01
225.7	482.1	0.990	3.52	2.13	0.06	0.03	0.02	0.01	0.01
225.7	321.3	0.982	4.35	1.41	0.05	0.03	0.02	0.02	0.01

Experimental results



Inductors used in the experimental results.
Left: $L = 1\ mH$ (RM12-3C90 core with $R_L = 0.25\ \Omega$).
Right: $L_2 = 1.5\ mH$ (soft saturation Kool mμ core with $R_{L2} = 0.35\ \Omega$)

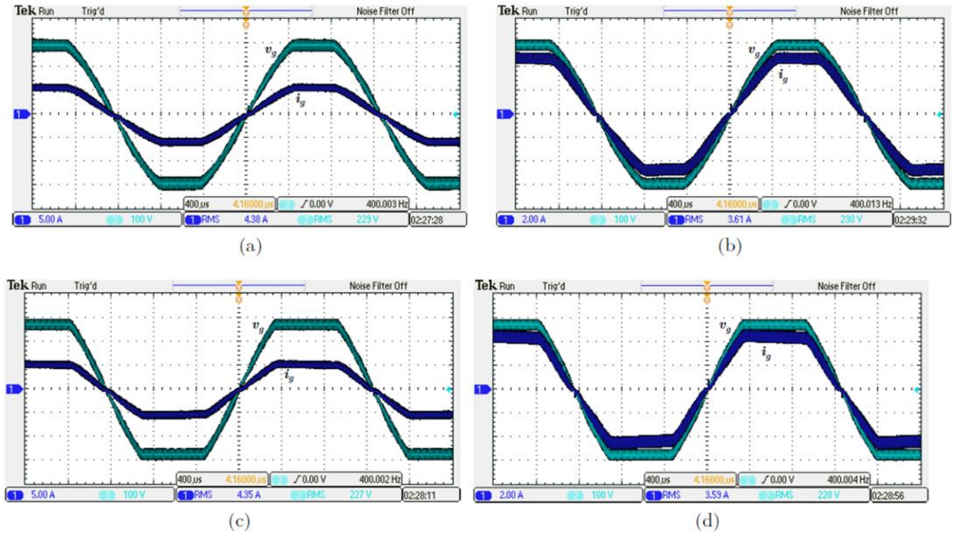


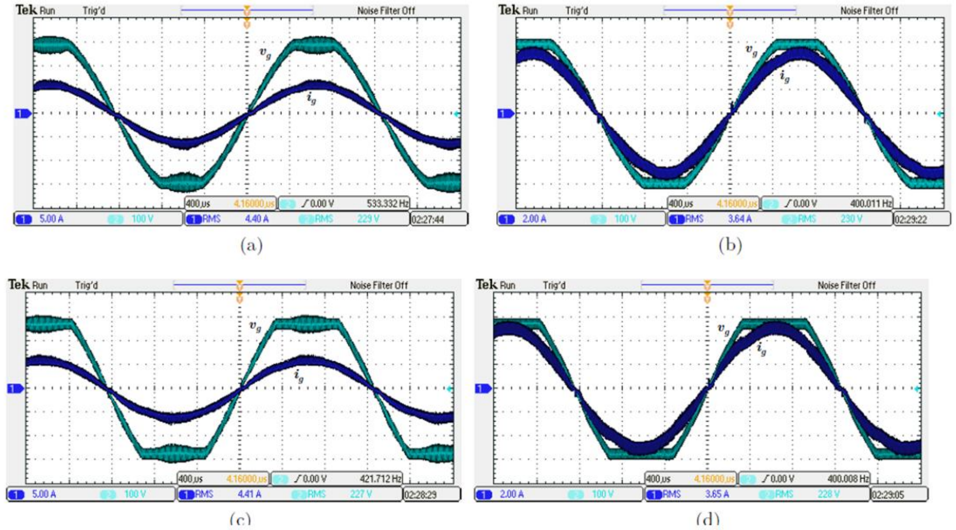
V_o = 400 V_{dc} and L_2 = 1.5mH (R_{L2} = 0.35 Ω).
(a) V_g = 230 V_{rms}(50Hz), P_g = 970W.
(b) V_g = 85 V_{rms}(60Hz), P_g = 320W.

Experimental results

Experimental results with $L_2 = 1.5\ mH$			
V_g	P_g	PF	$THDi$
250	460 W	0.975	9.0 %
	645 W	0.991	8.5 %
	800 W	0.993	9.5 %
	970 W	0.993	10.5 %
230	460 W	0.984	8.1 %
	640 W	0.988	9.1 %
	800 W	0.992	9.8 %
	970 W	0.993	10.5 %
180	323 W	0.980	5.4 %
	485 W	0.989	7.1 %
	650 W	0.992	8.6 %
	820 W	0.991	10.5 %
120	497 W	0.996	9.8 %
	323 W	0.988	9.8 %
	497 W	0.996	9.8 %
85	161 W	0.989	5.0 %
	336 W	0.993	9.0 %

Experimental results





Resistance emulator under different power levels and input voltage distortions.
$V_g = 230\ V$, $f_{sw} = 96\ kHz$.
With *THDv* =5 % at (a) P_g =966.7 W and (b) P_g =800.6 W.
With *THDv* =12 % at (c) P_g =965.1 W and (d) P_g =800.9 W.

Sinusoidal behavior under different power levels and input voltage distortions.
$V_g = 230\ V$, $f_{sw} = 96\ kHz$.
With *THDv* =5 % at (a) P_g =964.9 W and (b) P_g =799.5 W.
With *THDv* =12 % at (c) P_g =963.1 W and (d) P_g =800.4 W.

Experimental results

Pure Sinusoidal behavior under distorted voltage										
V_g (V)	P_g (W)	PF	$THDv$ (%)	$THDi$ (%)	I_1 (A)	I_3 (A)	I_5 (A)	I_7 (A)	I_9 (A)	I_{11} (A)
224.8	964.9	0.993	5.05	1.52	4.31	0.03	0.03	0.03	0.02	0.01
225.6	799.5	0.994	5.03	1.81	3.56	0.04	0.04	0.02	0.01	0.01
224.7	963.1	0.990	12.16	3.60	4.32	0.13	0.07	0.02	0.03	0.01
225.5	800.4	0.988	12.17	2.93	3.58	0.06	0.07	0.03	0.03	0.02

Resistance behavior (traditional PFC controller approach)										
V_g (V)	P_g (W)	PF	$THDv$ (%)	$THDi$ (%)	I_1 (A)	I_3 (A)	I_5 (A)	I_7 (A)	I_9 (A)	I_{11} (A)
224.7	966.7	0.996	4.93	4.38	4.30	0.12	0.14	0.03	0.03	0.04
225.6	800.6	0.995	4.92	4.64	3.55	0.11	0.12	0.03	0.02	0.03
224.7	965.1	0.995	11.95	11.25	4.28	0.41	0.16	0.08	0.02	0.01
225.5	800.9	0.995	11.95	11.25	3.53	0.37	0.14	0.07	0.02	0.01

Future works

- To extend the Sensorless PFC controller with current rebuilding to other topologies
  - SEPIC
  - Bridgeless and bidirectional Boost PFC rectifiers
  - Three phase bidirectional converters
- Investigate the use of time high resolution modulator
- Incorporate notch filter action in the voltage loop
- Investigate other parameters to achieve the feedback compensation of estimation errors
- Increase the speed of the feedback compensation
- Investigate the use of autotuning circuits
- Improve the PF in DCM

Conclusions

- Active error compensation is required to achieve universal current sensorless controllers
- Extrapolation of voltage data and time feedforward compensation can achieve a satisfactory power factor under limited and static input voltage and load conditions
- Continuous feedforward compensation is required because the switching delays depend on the devices and temperature
- Feedforwad time compensation can also compensate for voltage acquisition errors
- Feedforward time compensation is fast but coarse and cannot reach the best power factor
- It is easy to increase the resolution of the compensation for the difference between the real and estimated $V \cdot s$ using the voltage variable instead of the time variable
- The error between the estimation and detection of the DCM is an adequate variable to achieve the compensation of $V \cdot s$ estimation errors
- Feedback compensation achieve satisfactory power factor at different loads and input voltage
- Combination of feedforward and feedback compensation achieve universal PFC controller without loosing much performance in transients
- The proposal requires no modification for different PFC design operating in CCM

Thank you !